IEI Integration Corp.

MODEL:

IMBAX-SP6

ATX Motherboard Supports AMD SP6 EPYC™ CPU, Six DDR5 RDIMM, M.2 M Key, PCIe Gen5/Gen4 x16, PCIe Gen4 x8, Eight SATA 6Gb/s, DisplayPort, USB 3.2 Gen 1, 2.5GbE LAN, TPM, and RoHS

User Manual

Rev. 1.00 – July 26, 2024

RoHS Lead Free

Revision

Date	Version	Changes
July 26, 2024	1.00	Initial release

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Manual Conventions

WARNING

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.

CAUTION

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.

NOTE

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.

HOT SURFACE

This symbol indicates a hot surface that should not be touched without taking care.

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Introduction

1.1 Introduction

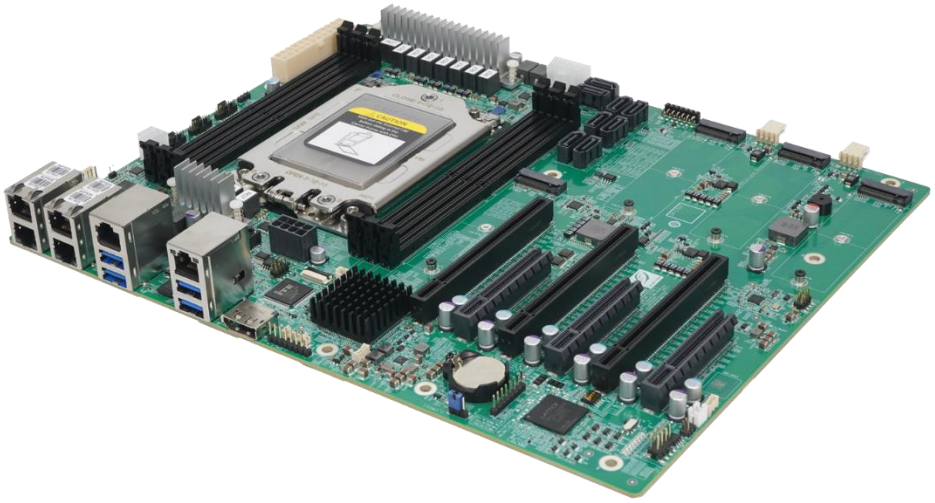


Figure 1-1: IMBAX-SP6

The IMBAX-SP6 is an ATX motherboard. It accepts a Socket SP6 AMD EPCY™ processor with 8 to 64 cores, and supports six 288-pin 4800 MHz DDR5 RDIMMs up to 576 GB.

The IMBAX-SP6 provides four 2.5GbE interfaces through the Intel® I225-LM/I226-LM PCIe controllers. In addition, it supports eight SATA 6Gb/s drives, and includes four M.2 M-key slots for installing NVMe SSDs.

Expansion and I/O include three PCIe x16 slots, three PCIe x8 slots, four USB 3.2 Gen 1 (5Gb/s) on the rear panel, two USB 2.0 by pin headers, one RS-232 RJ-45 console port, and one DisplayPort connector. Moreover, the on-board AST2600 controller enhances the motherboard with IPMI functionality, enabling remote monitoring and management of the system.

1.2 Features

Some of the IMBAX-SP6 motherboard features are listed below:

- ATX form factor
- Socket SP6 AMD EPCY™ processor supporting 8 to 64 cores
- Six 288-pin 4800 MHz DDR5 ECC RDIMM slots, up to 576 GB
- Four Intel® PCIe 2.5GbE connectors
- Eight SATA 6Gb/s ports
- Four M.2 2242/2280 M-key slots support NVMe SSDs via PCIe x4
- Four USB 3.2 Gen 1 (5Gb/s) and two USB 2.0
- Three PCIe x16 slots and three PCIe x8 slots
- One RS-232 console port (via RJ-45 connector)
- On-board AST2600 controller supporting IPMI
- RoHS compliant

1.3 Connectors

The connectors on the IMBAX-SP6 are shown in the figure below.

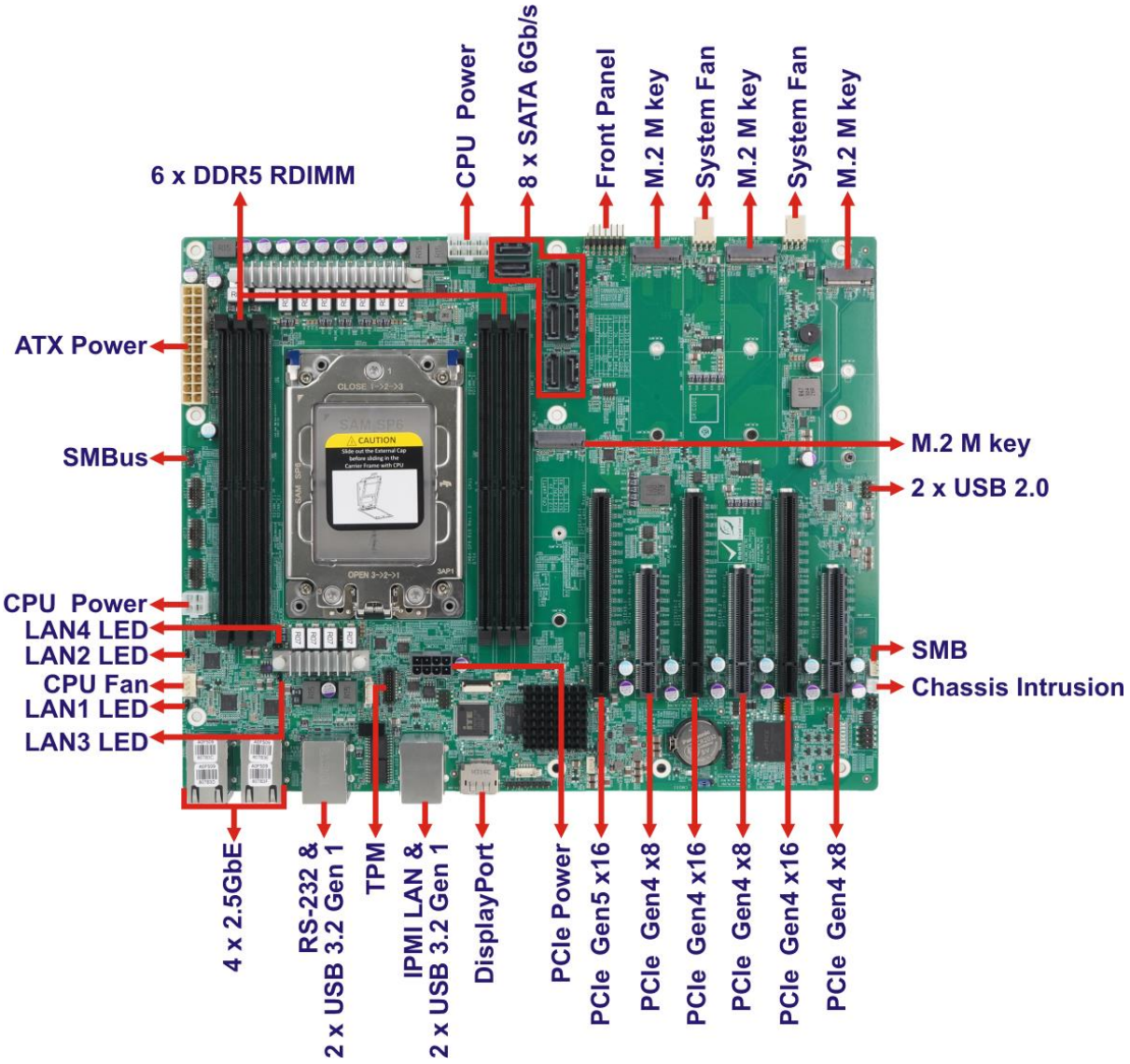


Figure 1-2: Connectors

1.4 Dimensions

The main dimensions of the IMBAX-SP6 are shown in the diagram below.

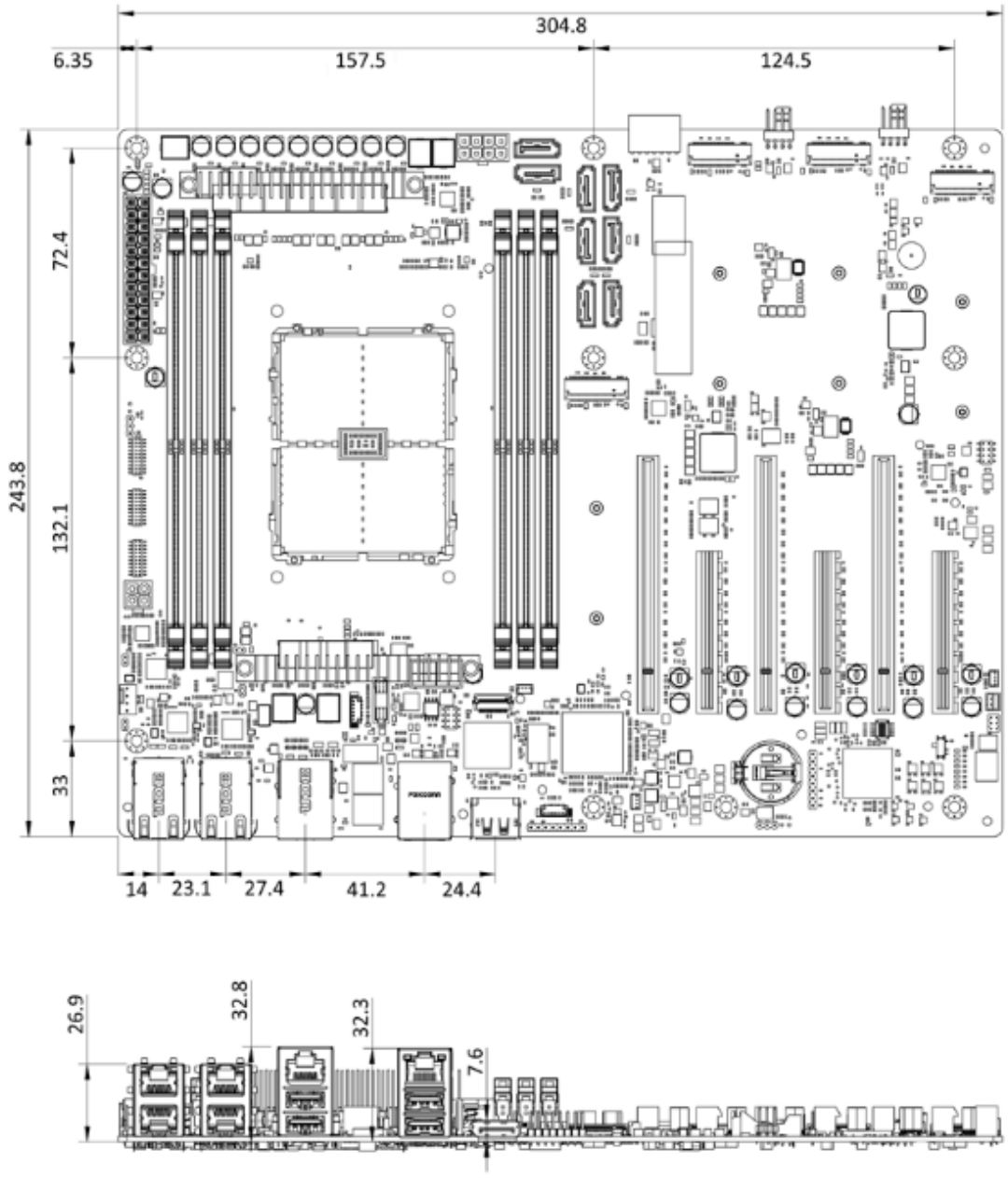


Figure 1-3: Dimensions (mm)

1.5 Data Flow

Figure 1-4 shows the data flow between the CPU and other components installed on the motherboard.

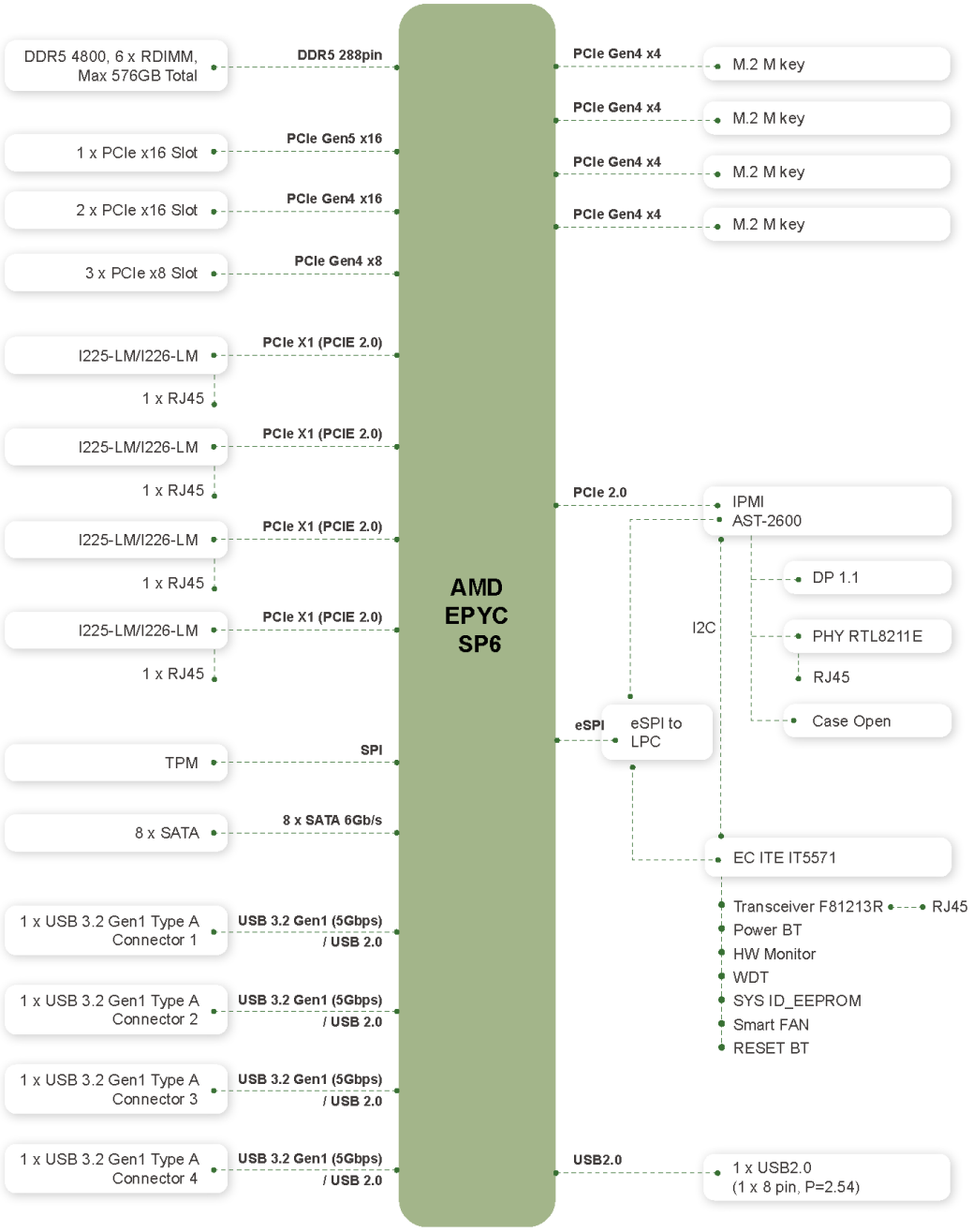


Figure 1-4: Data Flow Diagram

1.6 Technical Specifications

The IMBAX-SP6 technical specifications are listed below.

Specification/Model	IMBAX-SP6
Form Factor	ATX
CPU Supported	Socket SP6 AMD EPCY™ processor, 8 to 64 cores
Memory	Six 288-pin 4800 MHz DDR5 ECC RDIMM slots (system max. 576 GB)
Display Output	One DisplayPort (1920x1080)
BIOS	AMI UEFI BIOS
Ethernet Controllers	Intel® I225-LM/I226-LM Ethernet controllers
IPMI	On-board AST2600 controller 1 x GbE RJ45 IPMI management port
Embedded Controller	IT5771
Watchdog Timer	Software programmable supports 1~255 sec. system reset
Expansions	1 x PCIe Gen5 x16 slot 2 x PCIe Gen4 x16 slots 3 x PCIe Gen4 x8 slots 4 x M.2 M key slots (2242/2280, PCIe Gen4 x4, support NVMe SSD)
I/O Interface Connectors	
Chassis Intrusion	One 2-pin wafer
Ethernet	Four RJ-45 2.5GbE ports
Fan	One 4-pin CPU fan connector Two 4-pin system fan connectors
Front Panel	One 14-pin header (power LED, HDD LED, speaker, power button, reset button)
SMB	One 4-pin wafer connector
LAN LEDs	Four 2-pin headers
Serial ATA	Eight SATA 6Gb/s connectors

Serial Ports	One external RS-232 console port (RJ-45)
USB 2.0	Two USB 2.0 ports via internal pin header
USB 3.2	Four USB 3.2 Gen 1 (5Gb/s) ports on rear panel
TPM	One TPM connector
Environmental and Power Specifications	
Power Supply	AT/ATX power supply Support AT/ATX mode
Power Consumption	5VSB@0.7A, 5V@1.68A, 3.3V@0.87A, 12V@9.4A (AMD EPYC™ 8534P processor with 192GB (six of 32GB) 4800MHz DDR5 memory)
Operating Temperature	0ºC ~ 60ºC
Storage Temperature	-30ºC ~ 70ºC
Operating Humidity	5% ~ 95% (non-condensing)
Safety & EMC	CE/FCC compliant
Physical Specifications	
Dimensions	244 mm x 305 mm
Weight (Net)	900 g

Table 1-1: IMBAX-SP6 Specifications

Chapter

2

Packing List

2.1 Anti-static Precautions

WARNING!

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

Make sure to adhere to the following guidelines:

- ***Wear an anti-static wristband***: Wearing an anti-static wristband can prevent electrostatic discharge.
- ***Self-grounding***: Touch a grounded conductor every few minutes to discharge any excess static buildup.
- ***Use an anti-static pad***: When configuring any circuit board, place it on an anti-static mat.
- ***Only handle the edges of the PCB***: Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

2.2 Unpacking Precautions

When the IMBAX-SP6 is unpacked, please do the following:

- Follow the anti-static guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.

2.3 Packing List

NOTE:

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the IMBAX-SP6 was purchased from or contact an IEI sales representative directly by sending an email to sales@ieiworld.com.

The IMBAX-SP6 is shipped with the following components:

Quantity	Item and Part Number	Image
1	IMBAX-SP6 single board computer	
2	SATA cable	
1	I/O shielding	
1	Quick installation guide	

Table 2-1: Packing List

Chapter

3

Connectors

3.1 Peripheral Interface Connectors

This chapter details all the peripheral interface connectors.

3.1.1 IMBAX-SP6 Layout

The figure below shows all the peripheral interface connectors.

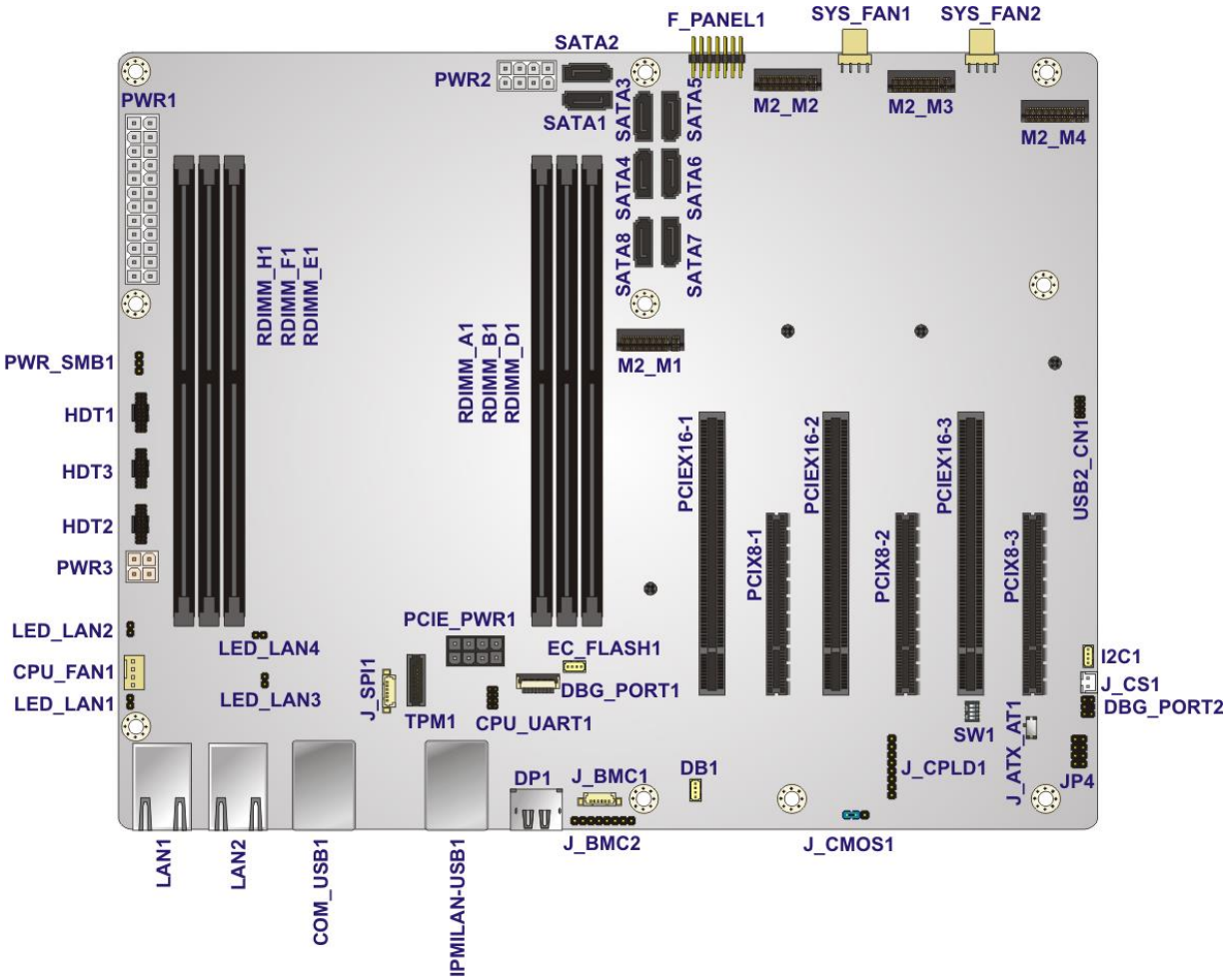


Figure 3-1: Peripheral Interface Connectors

3.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

Connector	Type	Label
ATX power connector	24-pin connector	PWR1
BMC JTAG connector	8-pn header	J_BMC2
Chassis intrusion connector	2-pin wafer	J_CS1
CPU debug connectors	20-pin header	HDT1, HDT2, HTD3
CPU power connector (1)	8-pin Molex connector	PWR2
CPU power connector (2)	4-pin Molex connector	PWR3
CPLD FW programming connector	8-pin header	J_CPLD1
CPLD debug connector	8-pin header	JP4
CPLD debug switch	4-position DIP switch	SW1
DDR5 RDIMM sockets	288-pin socket	RDIMM_A1, RDIMM_B1, RDIMM_D1, RDIMM_E1, RDIMM_F1, RDIMM_H1
Debug 80/81 port	6-pin header	DBG_PORT2
Fan connector (CPU)	4-pin wafer	CPU_FAN1
Fan connectors (system)	4-pin wafer	SYS_FAN1, SYS_FAN2
Front panel connector	14-pin header	F_PANEL1
LAN LED connectors	2-pin header	LED_LAN1, LED_LAN2, LED_LAN3, LED_LAN4

Connector	Type	Label
PCIe x16 slots	PCIe x16 slot	PCIEX16-1, PCIEX16-2, PCIEX16-3
PCIe x8 slots	PCIe x8 slot	PCIEX8-1, PCIEX8-2, PCIEX8-3
PCIe power connector	8-pin connector	PCIE_PWR1
SATA 6Gb/s drive connectors	7-pin SATA connector	SATA1, SATA2, SATA3, SATA4, SATA5, SATA6, SATA7, SATA8
SMBus connector	4-pin wafer	I2C1
SMBus connector for EC FW	4-pin wafer	EC_FLASH1
SMBus connector for power FW	3-pin header	PWR_SMB1
SPI flash connector, BIOS	6-pin wafer	J_SPI1
SPI flash connector, BMC FW	6-pin wafer	J_BMC1
TPM connector	20-pin header	TPM1
USB 2.0 connector	8-pin header	USB2_CN1
CPU UART debug port for internal use	8-pin header	CPU_UART1
EC debug port for internal use	20-pin FPC	DBG_PORT1
BMC UART debug port for internal use	4-pin wafer	DB1

Table 3-1: Peripheral Interface Connectors

3.1.3 External Interface Panel Connectors

The table below lists the connectors on the external I/O panel.

Connector	Type	Label
2.5GbE connectors	Dual-port RJ-45 LAN	LAN1, LAN2
RS-232 and USB 3.2 Gen 1 connector	RJ-45 & USB 3.2 Gen 1 combo	COM1_USB1
IPMI LAN and USB 3.2 Gen 1 connector	RJ-45 & USB 3.2 Gen 1 combo	IPMILAN-USB1
DisplayPort connector	DisplayPort	DP1

Table 3-2: Rear Panel Connectors

3.2 Internal Peripheral Connectors

The section describes all of the connectors on the IMBAX-SP6.

3.2.1 ATX Power Connector

CN Label: **PWR1**

CN Type: 24-pin connector, p=4.2 mm

CN Location: See **Figure 3-2**

CN Pinouts: See **Table 3-3**

The ATX power connector connects to an ATX power supply.

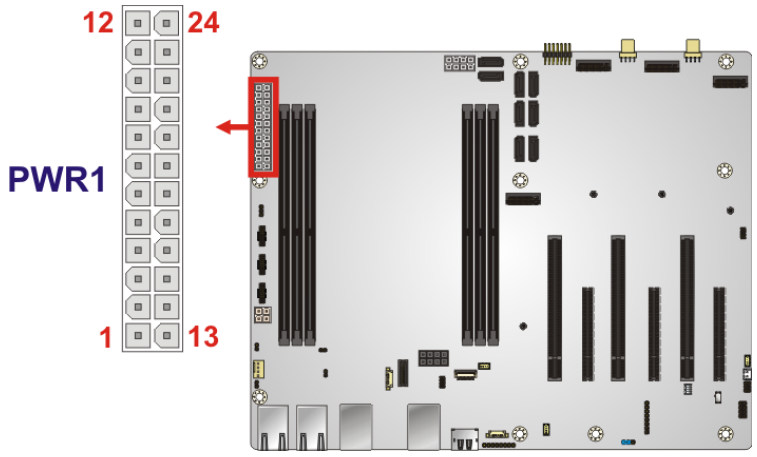


Figure 3-2: ATX Power Connector Location

Pin	Description	Pin	Description
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	GND	15	GND
4	+5V	16	PS_ON
5	GND	17	GND
6	+5V	18	GND
7	GND	19	GND
8	Power good	20	-5V
9	5VSB	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	GND

Table 3-3: ATX Power Connector Pinouts

3.2.2 BMC JTAG Connector

CN Label: **J_BMC2**

CN Type: 8-pin header, p=2.54 mm

CN Location: See **Figure 3-3**

CN Pinouts: See **Table 3-4**

The BMC JTAG connector can be used for BMC debug.

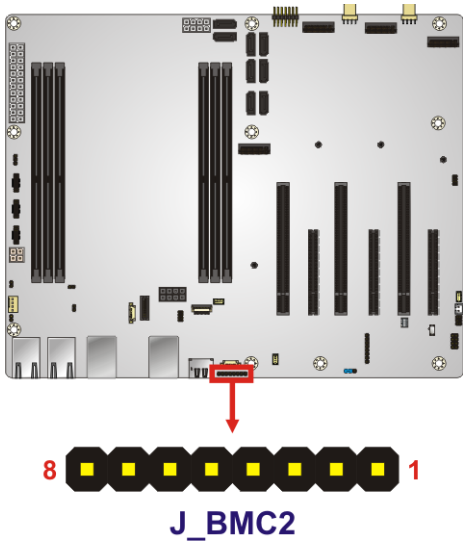


Figure 3-3: BMC JTAG Connector Location

Pin	Description	Pin	Description
1	+3.3V_BMC	5	N/C
2	ARM_TDO	6	ARM_TMS
3	ARM_TDI	7	GND
4	N/C	8	ARM_TCK

Table 3-4: BMC JTAG Connector Pinouts

3.2.3 Chassis Intrusion Connector

CN Label: **J_CS1**

CN Type: 2-pin wafer, p=2.0 mm

CN Location: See **Figure 3-4**

CN Pinouts: See **Table 3-5**

The chassis intrusion connector is for a chassis intrusion detection sensor or switch that detects if a chassis component is removed or replaced.

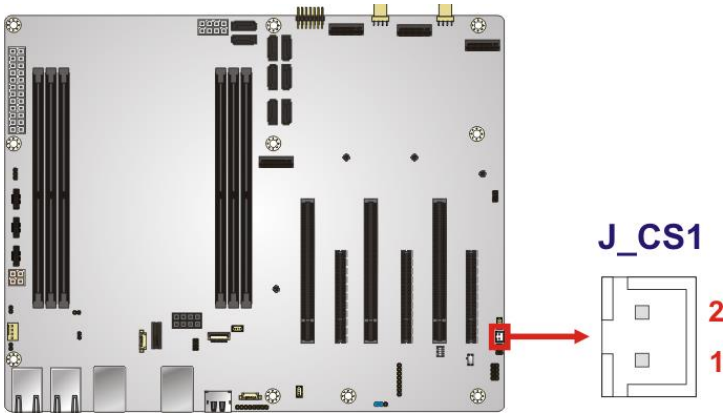


Figure 3-4: Chassis Intrusion Connector Location

Pin	Description
1	CASEOPEN_N
2	GND

Table 3-5: Chassis Intrusion Connector Pinouts

3.2.4 CPU Debug Connectors

CN Label: **HDT1, HDT2, HDT3**

CN Type: 20-pin header, p=1.27 mm

CN Location: See **Figure 3-5**

CN Pinouts: See **Table 3-6**

Use these connectors for AMD CPU debug.

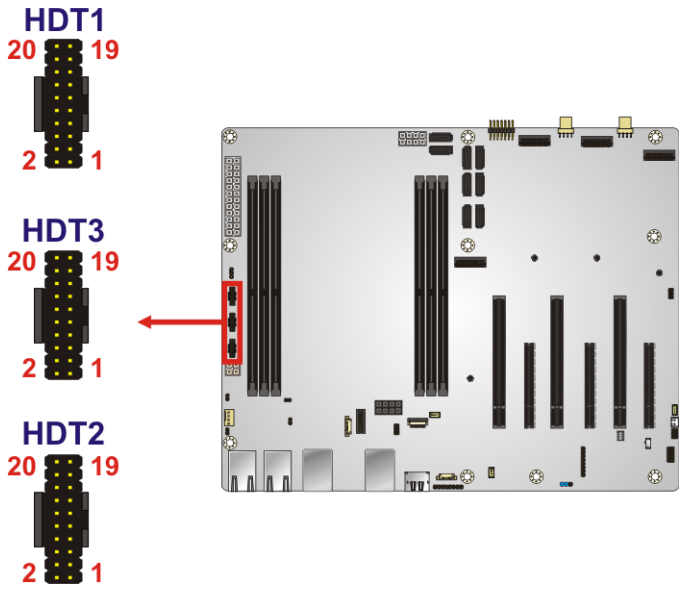


Figure 3-5: CPU Debug Connector Locations

Pin	Description	Pin	Description
1	+1.8V	2	HDT_TCK
3	GND	4	HDT_TMS
5	GND	6	HDT_TDI
7	GND	8	HDT_TDO
9	HDT_TRST_L	10	HDT_CONN_PWROK
11	XTRIG_L<6>	12	HDT_CONN_RESET_L
13	XTRIG_L<7>	14	N/C
15	XTRIG_L<5>	16	HDT_DBREQ_L
17	GND	18	HDT_CONN_TESTEN
19	+1.8V	20	N/C

Table 3-6: CPU Debug Connector Pinouts (HDT1)

Pin	Description	Pin	Description
1	+1.8V	2	HDT_TCK
3	GND	4	HDT_TMS
5	GND	6	G_CONN_HDT_TDOI
7	GND	8	HDT_TDO
9	HDT_TRST_L	10	N/C
11	XTRIG_L<6>	12	N/C
13	XTRIG_L<7>	14	N/C
15	XTRIG_L<5>	16	HDT_DBREQ_L
17	GND	18	P-HDT_CONN_TESTEN
19	+1.8V	20	N/C

Table 3-7: CPU Debug Connector Pinouts (HDT2)

Pin	Description	Pin	Description
1	+1.8V	2	HDT_TCK
3	GND	4	HDT_TMS
5	GND	6	HDT_TDO
7	GND	8	HDT_TDI
9	HDT_TRST_L	10	N/C
11	XTRIG_L<6>	12	N/C
13	XTRIG_L<7>	14	N/C
15	XTRIG_L<5>	16	HDT_DBREQ_L
17	GND	18	G-HDT_CONN_TESTEN
19	+1.8V	20	N/C

Table 3-8: CPU Debug Connector Pinouts (HDT3)

3.2.5 CPU Power Connector (1)

CN Label: **PWR2**

CN Type: 8-pin Molex power connector, p=4.2 mm

CN Location: See **Figure 3-6**

CN Pinouts: See **Table 3-9**

This connector provides power to the CPU.

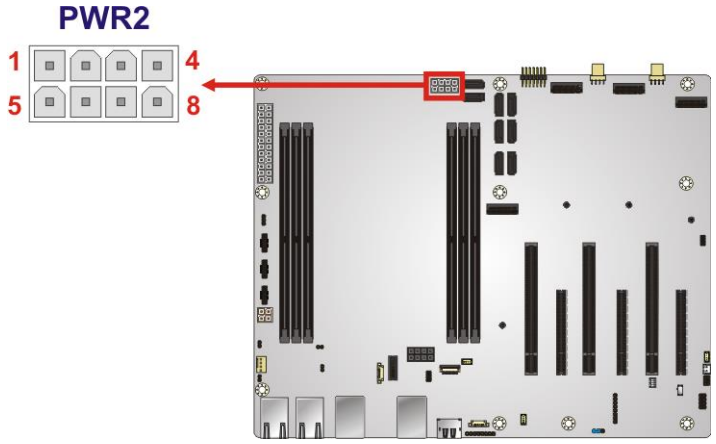


Figure 3-6: CPU Power Connector Pinout Location

Pin	Description	Pin	Description
1	GND	5	+12V
2	GND	6	+12V
3	GND	7	+12V
4	GND	8	+12V

Table 3-9: CPU Power Connector Pinouts

3.2.6 CPU Power Connector (2)

CN Label: **PWR3**

CN Type: 4-pin Molex power connector, p=4.2 mm

CN Location: See **Figure 3-7**

CN Pinouts: See **Table 3-10**

This connector provides power to the CPU.

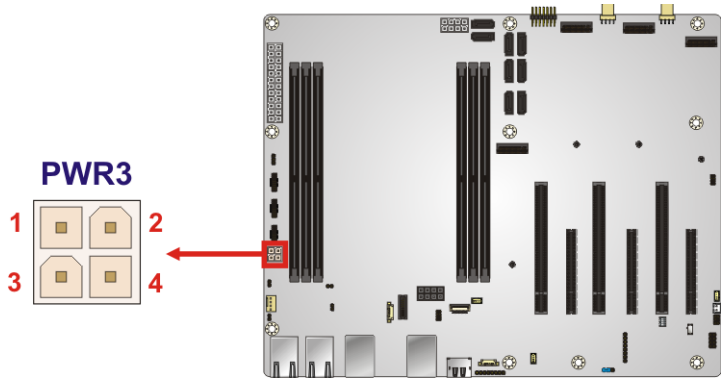


Figure 3-7: CPU Power Connector Pinout Location

Pin	Description	Pin	Description
1	GND	3	+12V
2	GND	4	+12V

Table 3-10: CPU Power Connector Pinouts

WARNING!

Shell must connect to PWR2 first, followed by PWR3.

PWR3 cannot be used independently without a prior connection to PWR2

3.2.7 CPLD Firmware Programming Connector

CN Label:	**J_CPLD1**
CN Type:	8-pin header, p=2.54 mm
CN Location:	See **Figure 3-8**
CN Pinouts:	See **Table 3-11**

Use this connector for CPLD firmware programming.

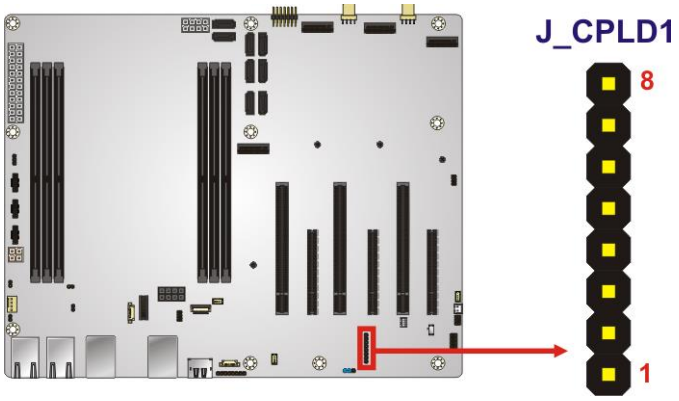


Figure 3-8: CPLD Firmware Programming Connector Location

Pin	Description
1	+3.3V_CPLD
2	CPLD_TDO
3	CPLD_TDI
4	N/C
5	N/C
6	CPLD_TMS
7	GND
8	CPLD_TCK

Table 3-11: CPLD Firmware Programming Connector Pinouts

3.2.8 CPLD Debug Connector and Switch

CN Label: **JP4, SW1**

CN Type: 8-pin header, p=2.54 mm & 4-position DIP switch

CN Location: See **Figure 3-9**

CN Pinouts: See **Table 3-12** & **Table 3-13**

The connector and the DIP switch are for CPLD debug.

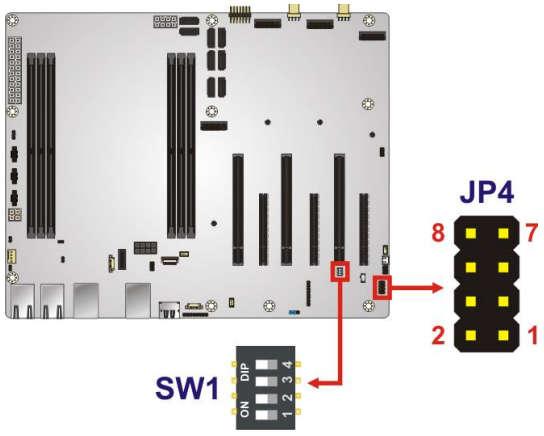


Figure 3-9: CPLD Debug Connector and Switch Location

Pin	Description	Pin	Description
1	FM_PLD_DEBUG0	2	FM_PLD_DEBUG4
3	FM_PLD_DEBUG1	4	FM_PLD_DEBUG5
5	FM_PLD_DEBUG2	6	FM_PLD_DEBUG6
7	FM_PLD_DEBUG3	8	FM_PLD_DEBUG7

Table 3-12: CPLD Debug Connector Pinouts

Pin	Description
1	CPLD_CONFIG0
2	CPLD_CONFIG1
3	CPLD_CONFIG2
4	CPLD_CONFIG3

Table 3-13: CPLD Debug Switch Settings

3.2.9 DDR5 RDIMM Sockets

CN Label:	**RDIMM_A1, RDIMM_B1, RDIMM_D1, RDIMM_E1, RDIMM_F1, RDIMM_H1**
CN Type:	288-pin DIMM socket
CN Location:	See **Figure 3-10**

The DIMM sockets are for DDR5 RDIMM memory modules.

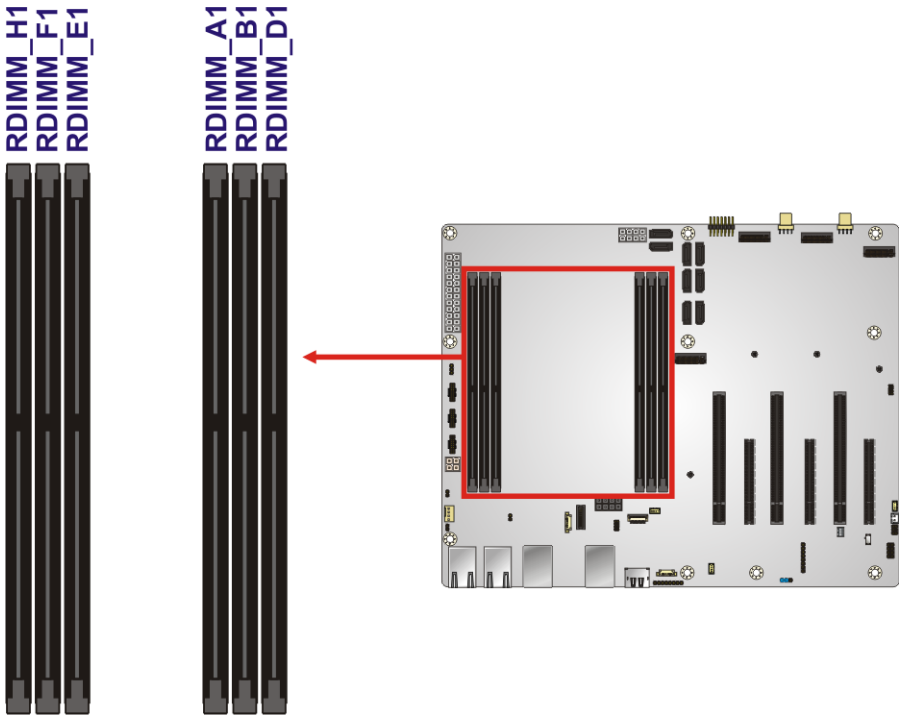


Figure 3-10: DDR5 RDIMM Socket Locations

3.2.10 Debug 80/81 Port

CN Label: **DBG_PORT2**

CN Type: 6-pin header, p=2.00 mm

CN Location: See **Figure 3-11**

CN Pinouts: See **Table 3-14**

The debug connector is used for system debug.

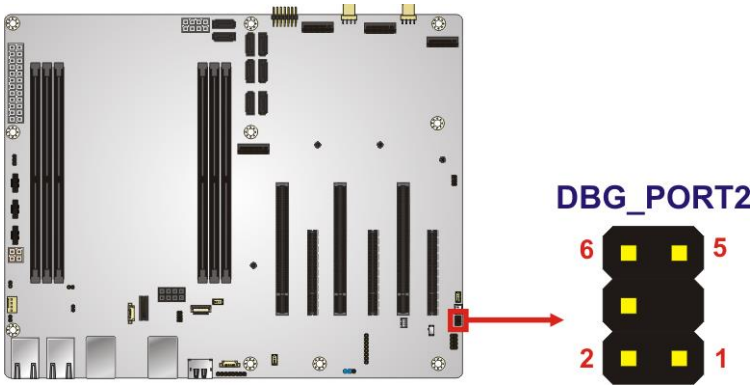


Figure 3-11: Debug 80/81 Port Location

Pin	Description	Pin	Description
1	VCC5V	2	SMCLK_EC
3	NC	4	SMDAT_EC
5	GND	6	RST#

Table 3-14: Debug 80/81 Port Pinouts

3.2.11 Fan Connector (CPU)

CN Label:	**CPU_FAN1**
CN Type:	4-pin wafer, p=2.54 mm
CN Location:	See **Figure 3-12**
CN Pinouts:	See **Table 3-15**

The fan connector attaches to a CPU cooling fan.

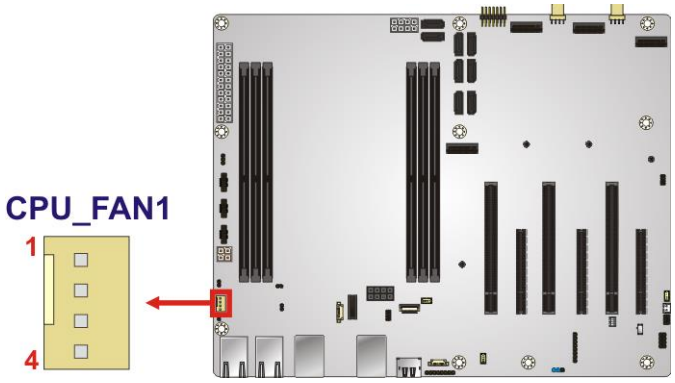


Figure 3-12: CPU Fan Connector Location

Pin	Description
1	GND
2	+12V
3	FANIO
4	PWM

Table 3-15: CPU Fan Connector Pinouts

3.2.12 Fan Connectors (System)

CN Label:	**SYS_FAN1, SYS_FAN2**
CN Type:	4-pin wafer, p=2.54 mm
CN Location:	See **Figure 3-13**
CN Pinouts:	See **Table 3-16**

Each fan connector attaches to a system cooling fan.

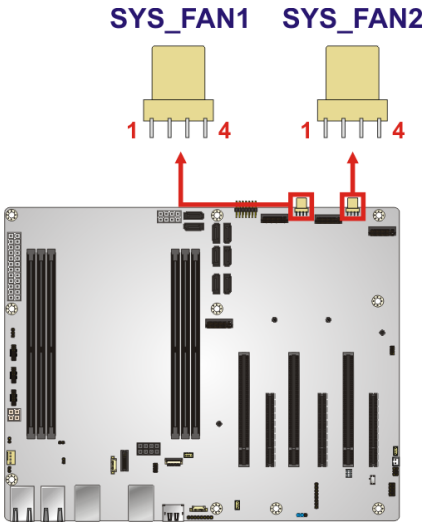


Figure 3-13: System Fan Connector Locations

Pin	Description
1	GND
2	+12V
3	FANIO
4	PWM

Table 3-16: System Fan Connector Pinouts

3.2.13 Front Panel Connector

CN Label: **F_PANEL1**

CN Type: 14-pin header, p=2.54 mm

CN Location: See **Figure 3-14**

CN Pinouts: See **Table 3-17**

The front panel connector connects to the indicator LEDs and buttons on the computer's front panel.

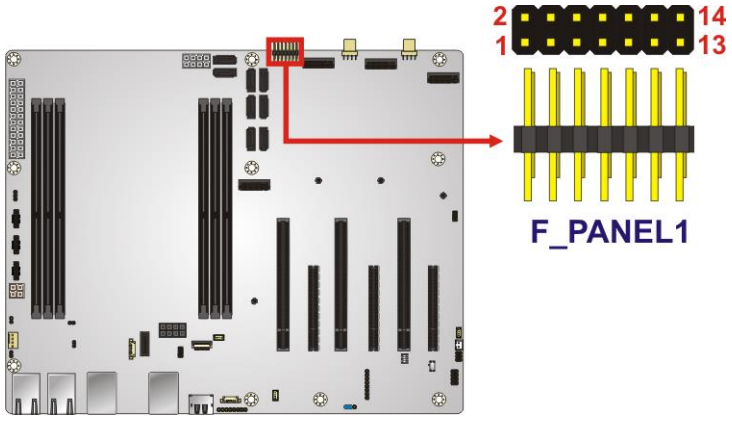


Figure 3-14: Front Panel Connector Location

Function	Pin	Description	Function	Pin	Description
Power LED	1	PWR_LED+	Speaker	2	Speaker+
	3	NC		4	NC
	5	PWR_LED-		6	NC
Power Button	7	PWR_BTN+		8	Speaker-
	9	PWR_BTN-		10	NC
HDD LED	11	HDD_LED+	Reset	12	Reset+
	13	HDD_LED-		14	Reset-

Table 3-17: Front Panel Connector Pinouts

3.2.14 LAN LED Connectors

CN Label:	**LED_LAN1, LED_LAN2, LED_LAN3, LED_LAN4**
CN Type:	2-pin header, p=2.00 mm
CN Location:	See **Figure 3-15**
CN Pinouts:	See **Table 3-18**

The LAN LED connectors are used to connect to the LAN LED indicators on the chassis to indicate users the link activities of the two LAN ports.

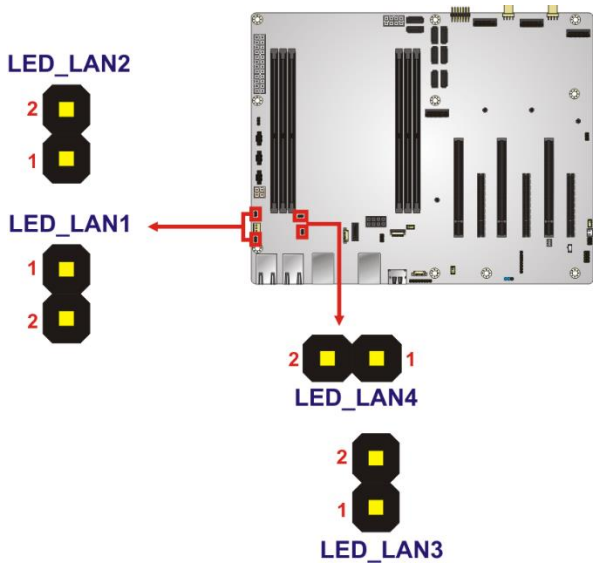


Figure 3-15: LAN LED Connector Locations

Pin	Description
1	+3.3V
2	LAN_LED_LINK#_ACT

Table 3-18: LAN LED Connector Pinouts

3.2.15 PCI Express x16 Slots

CN Label:	**PCIEX16-1, PCIEX16-2, PCIEX16-3**
CN Type:	PCIe x16 slot
CN Location:	See **Figure 3-16**

The PCIe x16 expansion card slots are for PCIe x16 expansion cards. The PCIEX16-1 slot provides PCIe Gen5 x16 signal while the PCIEX16-2 and the PCIEX16-3 slots provide PCIe Gen4 x16 signal.

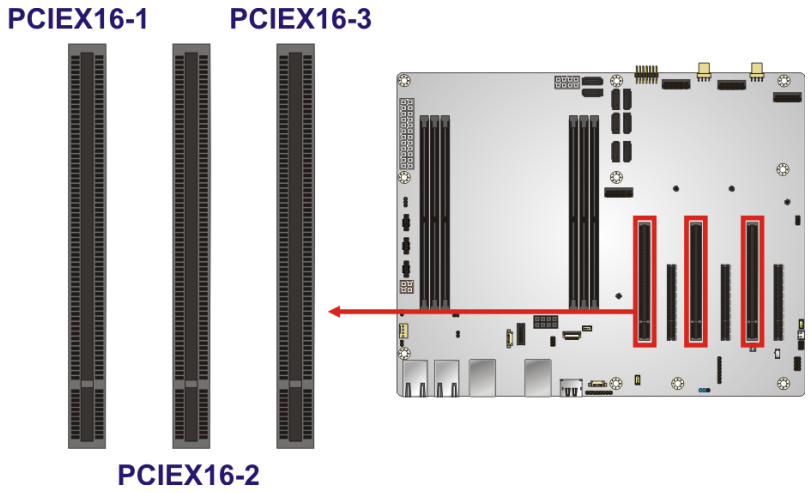


Figure 3-16: PCIe x16 Slot Locations

3.2.16 PCI Express x8 Slots

CN Label: **PCIEX8-1, PCIEX8-2, PCIEX8-3**

CN Type: PCIe x8 slot

CN Location: See **Figure 3-17**

The PCIe x8 expansion card slots are for PCIe Gen4 x8 expansion cards.

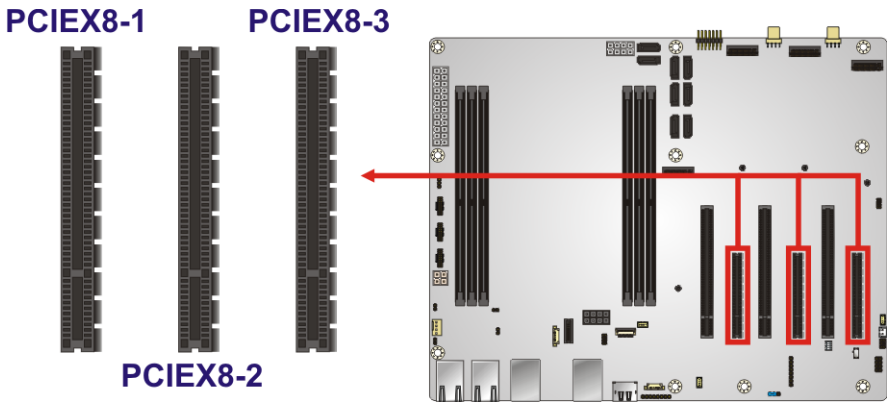


Figure 3-17: PCIe x8 Slot Location

3.2.17 PCIe Power Connector

CN Label: **PCIE_PWR1**

CN Type: 8-pin connector, p=4.20 mm

CN Location: See **Figure 3-18**

CN Pinouts: See **Table 3-19**

The PCIe power connector provides +12V power for PCIe cards.

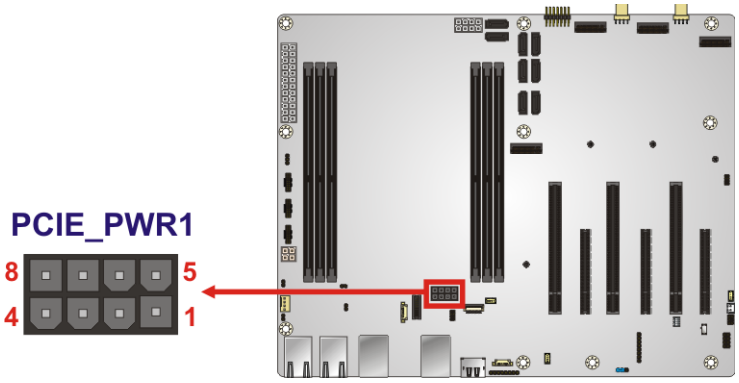


Figure 3-18: PCIe Power Connector Location

Pin	Description	Pin	Description
1	+12V	5	GND
2	+12V	6	GND
3	+12V	7	GND
4	GND	8	GND

Table 3-19: PCIe Power Connector Pinouts

3.2.18 SATA 6Gb/s Drive Connector

CN Label:	**SATA1, SATA2, SATA3, SATA4, SATA5, SATA6, SATA7, SATA8**
CN Type:	7-pin SATA drive connector
CN Location:	See **Figure 3-19**
CN Pinouts:	See **Table 3-20**

The SATA drive connectors can be connected to SATA drives and support up to 6Gb/s data transfer rate.

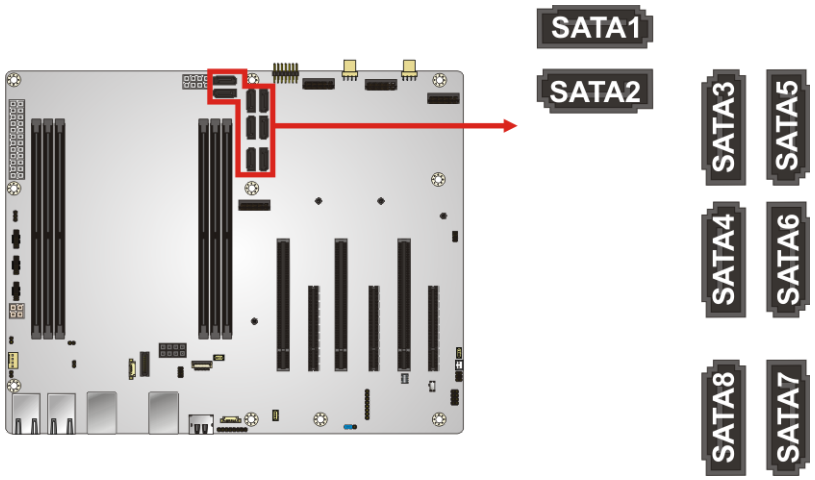


Figure 3-19: SATA 6Gb/s Drive Connector Locations

Pin	Description
1	GND
2	SATA_TX+
3	SATA_TX-
4	GND
5	SATA_RX-
6	SATA RX+
7	GND

Table 3-20: SATA 6Gb/s Drive Connector Pinouts

3.2.19 SMBus Connector

CN Label:	**I2C1**
CN Type:	4-pin wafer, p=1.25 mm
CN Location:	See **Figure 3-20**
CN Pinouts:	See **Table 3-21**

The SMBus (System Management Bus) connector provides low-speed system management communications.

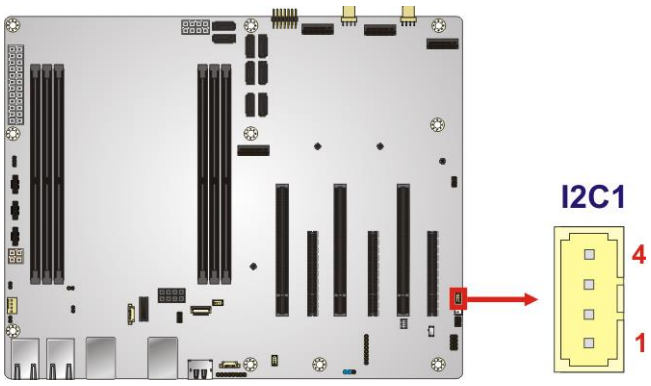


Figure 3-20: SMBus Connector Location

Pin	Description
1	GND
2	EC_SMDAT2
3	EC_SMCLK2
4	+V3.3A_EC

Table 3-21: SMBus Connector Pinouts

3.2.20 SMBus EC FW Programming Connector

CN Label: **EC_FLASH1**

CN Type: 4-pin wafer, p=1.25 mm

CN Location: See **Figure 3-21**

CN Pinouts: See **Table 3-22**

The connector is for EC firmware programming.

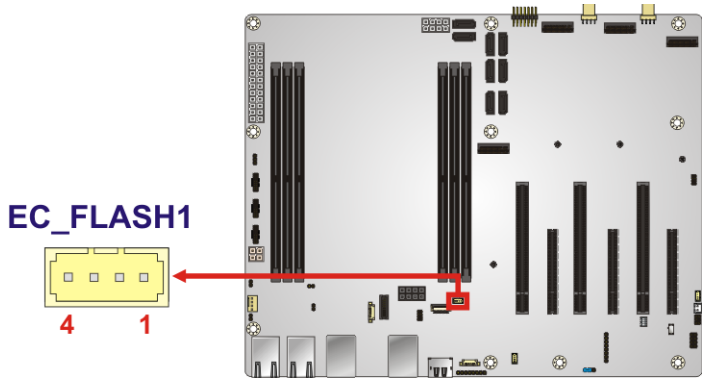


Figure 3-21: SMBus EC FW Programming Connector Location

Pin	Description
1	GND
2	I2C_DATA
3	I2C_CLK
4	NC

Table 3-22: SMBus EC FW Programming Connector Pinouts

3.2.21 SMBus Power FW Programming Connector

CN Label:	**PWR_SMB1**
CN Type:	3-pin header, p=2.54 mm
CN Location:	See **Figure 3-22**
CN Pinouts:	See **Table 3-23**

The connector is for power firmware programming.

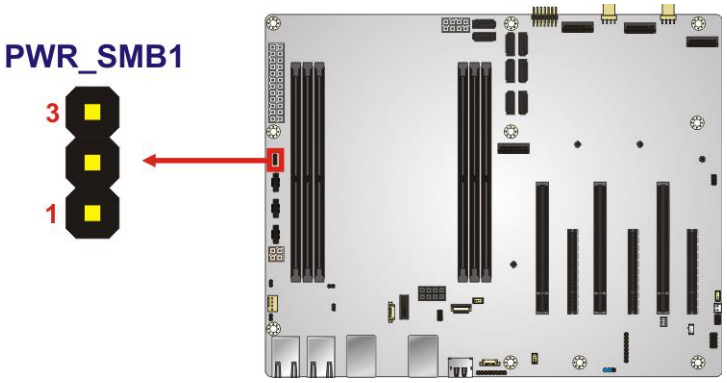


Figure 3-22: SMBus Power FW Programming Connector Location

Pin	Description
1	SCL
2	SDA
3	GND

Table 3-23: SMBus Power FW Programming Connector Pinouts

3.2.22 SPI Flash Connector, BIOS

CN Label: **J_SPI1**

CN Type: 6-pin wafer, p=1.25 mm

CN Location: See **Figure 3-23**

CN Pinouts: See **Table 3-24**

The SPI flash connector is used to flash the BIOS SPI ROM.

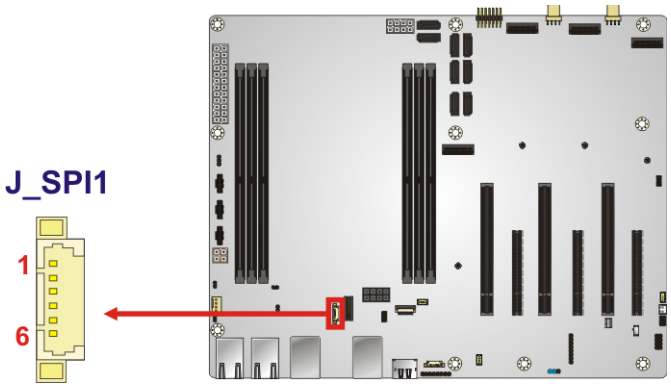


Figure 3-23: SPI Flash Connector Location

Pin	Description	Pin	Description
1	+3.3V	4	SPI_CLK
2	SPI_CS#	5	SPI_SI
3	SPI_SO	6	GND

Table 3-24: SPI Flash Connector Pinouts

3.2.23 SPI Flash Connector, EC

CN Label: **J_BMC1**

CN Type: 6-pin wafer, p=1.25 mm

CN Location: See **Figure 3-24**

CN Pinouts: See **Table 3-25**

The SPI flash connector is used to flash the BMC firmware.

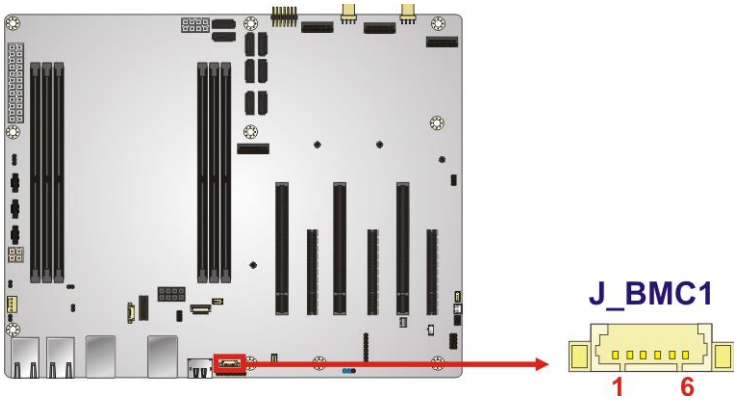


Figure 3-24: SPI BMC Flash Connector Location

Pin	Description	Pin	Description
1	+3.3V	4	SPI_CLK
2	SPI_CS#	5	SPI_SI
3	SPI_SO	6	GND

Table 3-25: SPI BMC Flash Connector Pinouts

3.2.24 TPM Connector

CN Label: **TPM1**

CN Type: 20-pin header, p=1.27 mm

CN Location: See **Figure 3-25**

CN Pinouts: See **Table 3-26**

The Trusted Platform Module (TPM) connector secures the system on bootup.

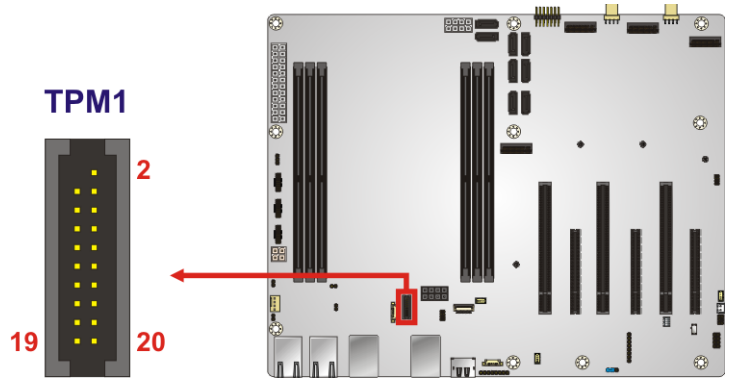


Figure 3-25: TPM Connector Pinout Location

Pin	Description	Pin	Description
		2	N/C
3	+1.8V	4	N/C
5	GND	6	+1.8V
7	SPI_TPM_CLK_SW	8	N/C
9	N/C	10	SPI_TPM_SO_SW
11	N/C	12	SPI_TPM_SI_SW
13	SPI_TPM_CS#_SW	14	GND
15	N/C	16	N/C
17	TPM_PIRQ_L	18	+1.8V
19	TPM_RST_L	20	N/C

Table 3-26: TPM Connector Pinouts

3.2.25 USB 2.0 Connector

CN Label:	**USB2_CN1**
CN Type:	8-pin header, p=2.00 mm
CN Location:	See **Figure 3-26**
CN Pinouts:	See **Table 3-27**

The USB 2.0 connector connects to USB 2.0 devices. Each pin header provides two USB 2.0 ports.

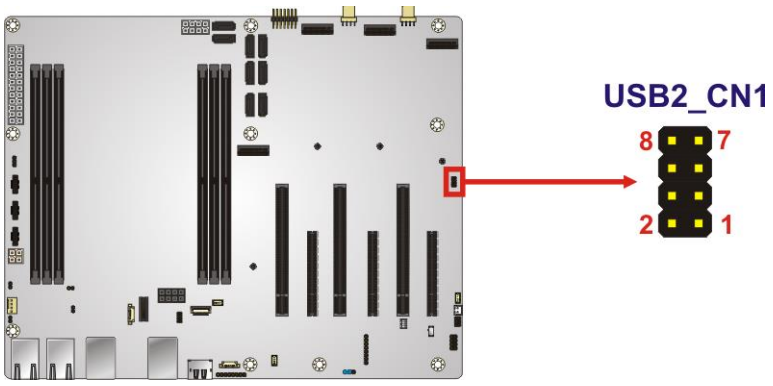


Figure 3-26: USB 2.0 Connector Pinout Location

Pin	Description	Pin	Description
1	VCC	2	GND
3	USB_DATA-	4	USB_DATA+
5	USB_DATA+	6	USB_DATA-
7	GND	8	VCC

Table 3-27: USB 2.0 Connector Pinouts

3.3 External Peripheral Interface Connector Panel

The figure below shows the external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:

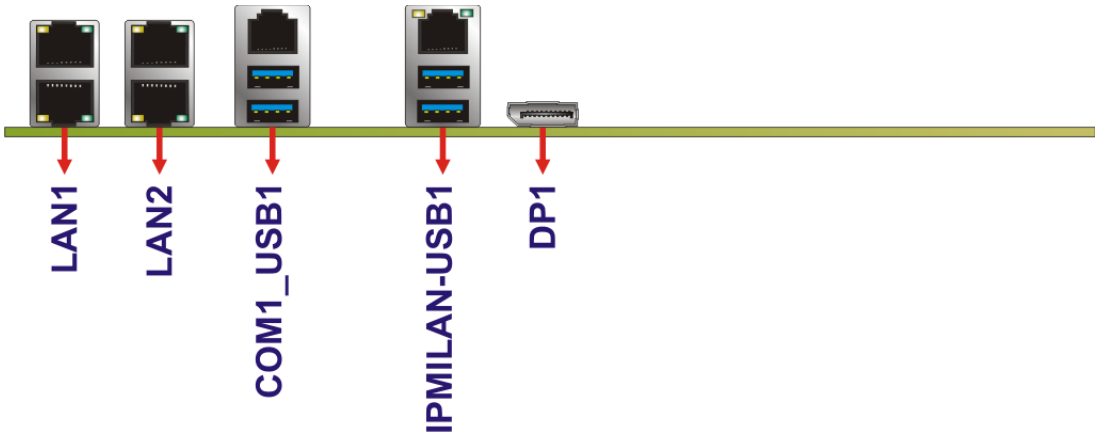


Figure 3-27: External Peripheral Interface Connectors

3.3.1 2.5GbE Connectors

CN Label: **LAN1, LAN2**

CN Type: RJ-45

CN Location: See **Figure 3-27**

CN Pinouts: See **Table 3-28**

A 100/1000/2500 Mb/s connection can be made to a Local Area Network.

Pin	Description	Pin	Description
1	MDIA0+	5	MDIA2-
2	MDIA0-	6	MDIA1-
3	MDIA1+	7	MDIA3+
4	MDIA2+	8	MDIA3-
LED	**Description**	**LED**	**Description**
A	on: linked blinking: data is being sent/received	B	off: 100 Mb/s orange: 1000 Mb/s green: 2500 Mb/s

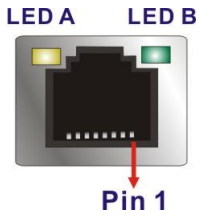


Table 3-28: 2.5GbE Connector Pinouts

NOTE:

Only the upper connector of the LAN1 port supports Wake-on-LAN (WOL), and the WOL function requires a minimum of 3A on the ATX Power +5VSB rail. If the current is lower than 3A, the WOL function may not work properly.

3.3.2 DisplayPort Connector

CN Label: **DP1**

CN Type: DisplayPort

CN Location: See **Figure 3-27**

CN Pinouts: See **Table 3-29**

The DisplayPort connector supports DisplayPort devices.

Pin	Description	Pin	Description
1	DATA_0P	11	GND
2	GND	12	DATA_3N
3	DATA_0N	13	CONFIG1
4	DATA_1P	14	CONFIG2
5	GND	15	AUX_P
6	DATA_1N	16	GND
7	DATA_2P	17	AUX_N
8	GND	18	DP_HPD
9	DATA_2N	19	GND
10	DATA_3P	20	DP_PWR

Table 3-29: DisplayPort Connector Pinouts

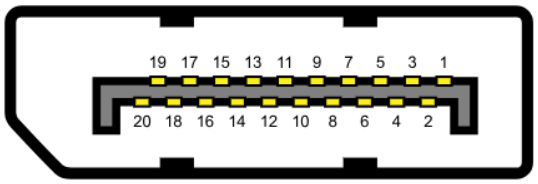


Figure 3-28: DisplayPort Connector Location

3.3.3 RS-232 and USB 3.2 Gen 1 Connectors

CN Label: **COM1_USB1**

CN Type: RJ-45 & USB 3.2 Gen 1 Type A combo

CN Location: See **Figure 3-27**

CN Pinouts: See **Table 3-30** and **Table 3-31**

The USB 3.2 Gen 1 (5Gb/s) connectors can be connected to USB 3.2 Gen 1 devices.

Pin	Description	Pin	Description
1	VCC	10	VCC
2	USB_DATA-	11	USB_DATA-
3	USB_DATA+	12	USB_ DATA+
4	GND	13	GND
5	USB3_RX-	14	USB3_RX-
6	USB3_RX+	15	USB3_ RX+
7	GND	16	GND
8	USB3_TX-	17	USB3_TX-
9	USB3_TX+	18	USB3_TX+

Table 3-30: USB 3.2 Gen 1 Port Pinouts

The RJ-45 serial port connects to a RS-232 serial communications device.

Pin	Description	Pin	Description
1	RTS	5	GND
2	DTR	6	SIN
3	SOUT	7	DSR
4	GND	8	CTS

Table 3-31: Serial Port Pinouts

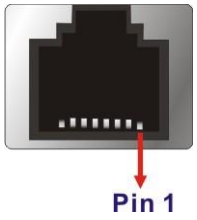


Figure 3-29: RJ-45 Serial Port Pinouts

3.3.4 IPMI LAN and USB 3.2 Gen 1 Connectors

CN Label: **IPMILAN-USB1**

CN Type: RJ-45 & USB 3.2 Gen 1 combo

CN Location: See **Figure 3-27**

CN Pinouts: See **Table 3-32** and **Table 3-30**

The RJ-45 connector of the IPMILAN_USB1 connector supports IPMI function.

Pin	Description	Pin	Description
1	MDIA0+	5	MDIA2-
2	MDIA0-	6	MDIA1-
3	MDIA1+	7	MDIA3+
4	MDIA2+	8	MDIA3-

Table 3-32: IPMI LAN Connector Pinouts

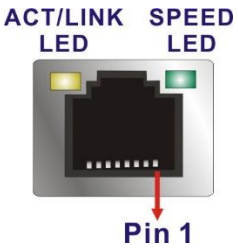


Figure 3-30: IPMI LAN Connector

Chapter

4

Installation

4.1 Anti-static Precautions

WARNING:

Failure to take ESD precautions during the installation of the IMBAX-SP6 may result in permanent damage to the IMBAX-SP6 and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the IMBAX-SP6. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the IMBAX-SP6 or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- ***Wear an anti-static wristband***: - Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- ***Self-grounding***:- Before handling the board touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- ***Use an anti-static pad***: When configuring the IMBAX-SP6, place it on an anti-static pad. This reduces the possibility of ESD damaging the IMBAX-SP6.
- ***Only handle the edges of the PCB***:-: When handling the PCB, hold the PCB by the edges.

4.2 Installation Considerations

NOTE:

The following installation notices and installation considerations should be read and understood before installation. All installation notices must be strictly adhered to. Failing to adhere to these precautions may lead to severe damage and injury to the person performing the installation.

WARNING:

The installation instructions described in this manual should be carefully followed in order to prevent damage to the components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
  - The user manual provides a complete description of the IMBAX-SP6 installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
  - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the IMBAX-SP6 on an anti-static pad:
  - When installing or configuring the motherboard, place it on an anti-static pad. This helps to prevent potential ESD damage.
- Turn all power to the IMBAX-SP6 off:
  - When working with the IMBAX-SP6, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the IMBAX-SP6, **DO NOT:**

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

4.3 Socket SP6 CPU Installation

WARNING:

CPUs are expensive and sensitive components. When installing the CPU please be careful not to damage it in anyway. Make sure the CPU is installed properly and ensure the correct cooling kit is properly installed.

DO NOT touch the pins at the bottom of the CPU. When handling the CPU, only hold it on the sides.

For detailed visual instructions on installing an AMD EPYC™ processor into Socket SP6, visit the official AMD YouTube channel and search for "How to Install AMD EPYC™ Processors".

4.4 DIMM Installation

CAUTION:

For multiple channel configuration, always install identical memory modules that feature the same capacity, timings, voltage, number of ranks and the same brand.

To install a DIMM, please follow the steps below and refer to **Figure 4-1**.

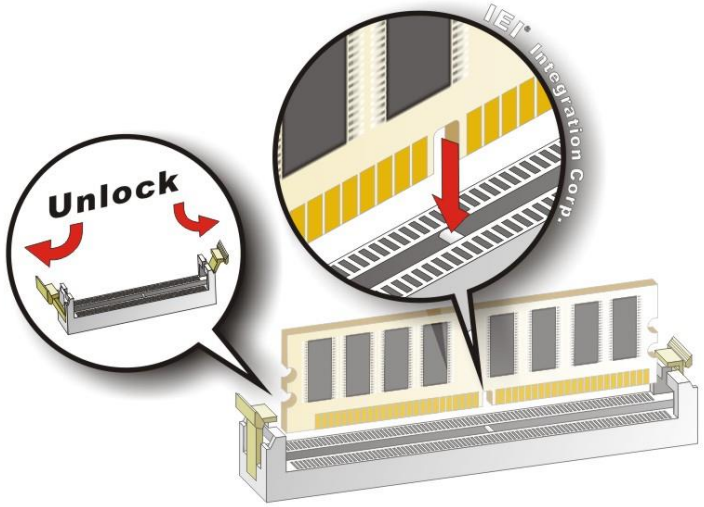


Figure 4-1: DIMM Installation

Step 1: **Open the DIMM socket handles**. Open the two handles outwards as far as they can. See **Figure 4-1**.

Step 2: **Align the DIMM with the socket**. Align the DIMM so the notch on the memory lines up with the notch on the memory socket. See **Figure 4-1**.

Step 3: **Insert the DIMM**. Once aligned, press down until the DIMM is properly seated. Clip the two handles into place. See **Figure 4-1**.

Step 4: To remove a DIMM, push both handles outward. The memory module is ejected by a mechanism in the socket.

4.5 M.2 Module Installation

To install an M.2 module, please follow the steps below.

Step 1: Locate the M.2 module slot. See **Chapter 3**.

Step 2: Remove the on-board retention screw as shown in **Figure 4-2**.

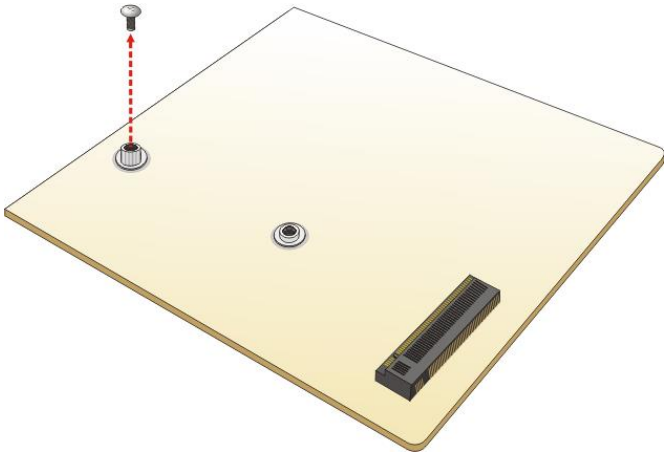


Figure 4-2: Removing the M.2 Module Retention Screw

Step 3: Line up the notch on the module with the notch on the slot. Slide the M.2 module into the socket at an angle of about 20º (Figure 4-3).

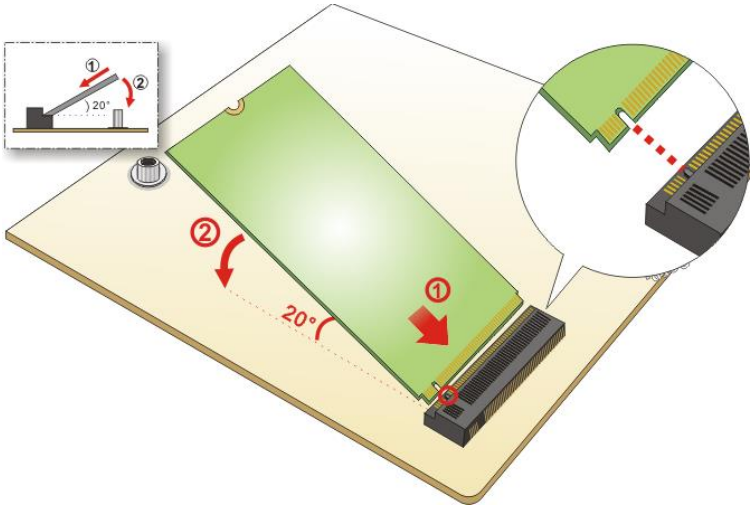


Figure 4-3: Inserting the M.2 Module into the Slot at an Angle

Step 4: Secure the M.2 module with an M2*3 retention screw (Figure 4-4).

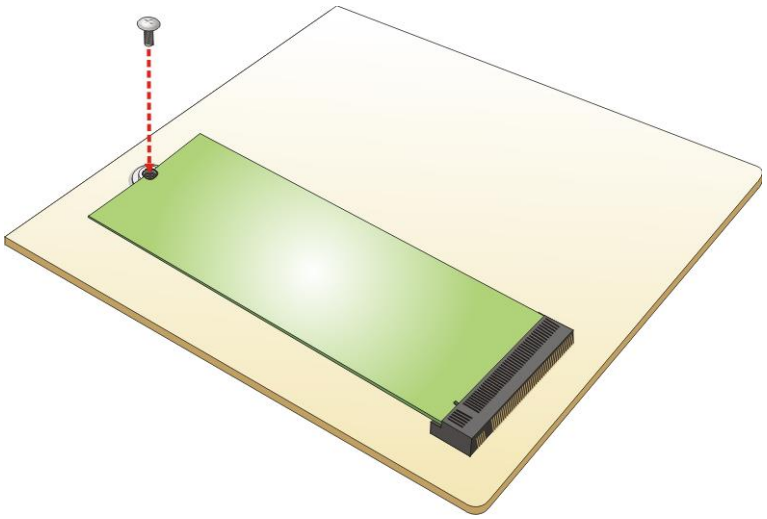
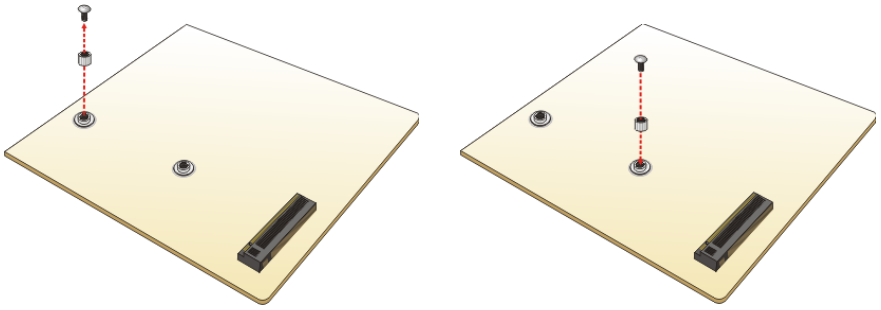


Figure 4-4: Securing the M.2 Module

NOTE:

For M.2 2242 modules, remove the pre-installed standoff from the M.2 2280 screw hole and install it in the designated M.2 2242 hole.



4.6 System Configuration

The system configuration should be performed before installation.

4.6.1 AT/ATX Power Mode Setting

The AT and ATX power mode selection is made through the AT/ATX power mode switch which is shown in **Figure 4-5**.

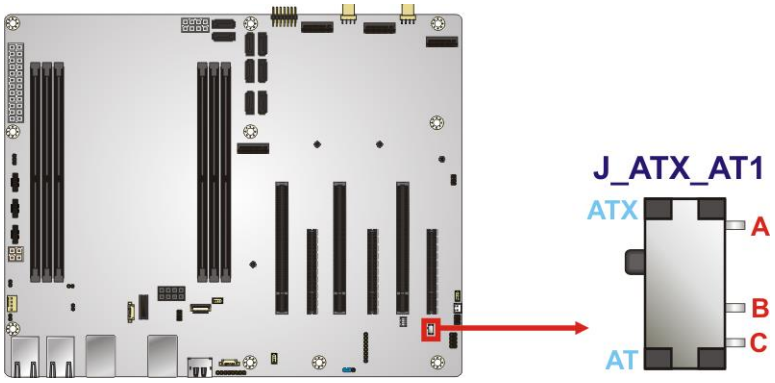


Figure 4-5: AT/ATX Power Mode Switch Location

Setting	Description
A-B	ATX power mode (default)
B-C	AT power mode

Table 4-1: AT/ATX Power Mode Switch Settings

4.6.2 Clear CMOS

To reset the BIOS, short the jumper for 3 seconds or more, then remove the jumper clip.

Setting	Description
Short 1-2	Keep current BIOS setup
Short 2-3	Clear BIOS

Table 4-2: Clear BIOS Jumper Settings

The location of the clear CMOS button (J_CMOS1) is shown in **Figure 4-6**.

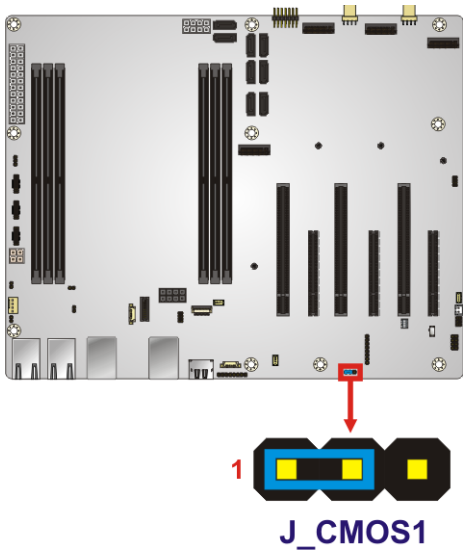


Figure 4-6: Clear CMOS Jumper Location

4.6.3 USB Power Selection

The USB power selection is made through the BIOS menu in “Chipset → PCH-IO Configuration”. Use the **USB Power SW1** and the **USB Power SW2** BIOS options to configure the correspondent USB ports (see **Table 4-3**) and refer to **Table 4-4** to select the USB power source.

BIOS Options	Configured USB Ports
USB Power SW1	IPMILAN-USB1B (external USB 3.2 Gen 1 ports)
USB Power SW2	COM1_USB1B (external USB 3.2 Gen 1 ports)

Table 4-3: BIOS Options and Configured USB Ports

Options	Description
+5V DUAL	+5V dual (default)
+5V	+5V

Table 4-4: USB Power Source Setup

Please refer to **Section 5.4.1** for detailed information.

4.7 Internal Peripheral Device Connections

This section outlines the installation of peripheral devices to the onboard connectors.

4.7.1 SATA Drive Connection

The IMBAX-SP6 is shipped with two SATA drive cables. To connect the SATA drives to the connectors, please follow the steps below.

Step 1: **Locate the connectors**. The locations of the SATA drive connectors are shown in **Chapter 3**.

Step 2: **Insert the cable connector**. Insert the cable connector into the on-board SATA drive connector until it clips into place. See **Figure 4-7**.

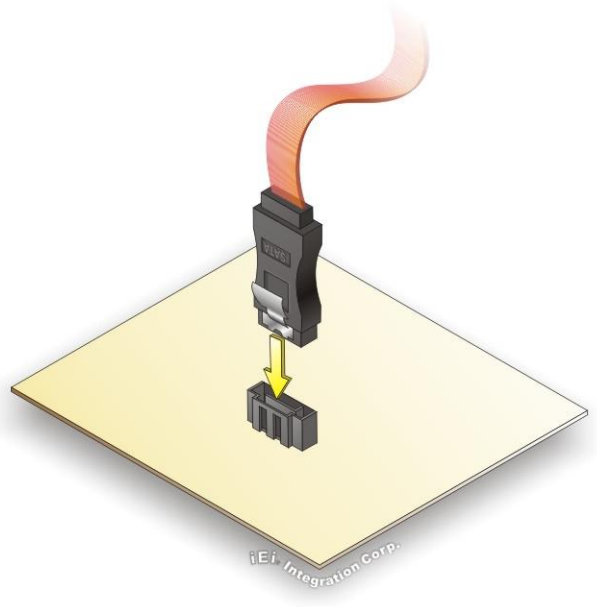


Figure 4-7: SATA Drive Cable Connection

Step 3: **Connect the cable to the SATA disk**. Connect the connector on the other end of the cable to the connector at the back of the SATA drive. See **Figure 4-8**.

Step 4: **Connect the SATA power cable**. Connect the SATA power connector to the back of the SATA drive. See **Figure 4-8**.

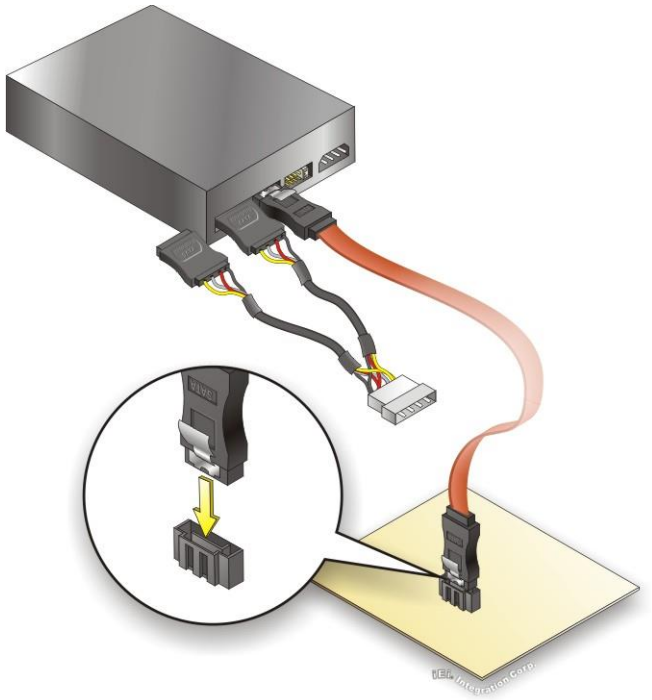


Figure 4-8: SATA Power Drive Connection

4.8 Driver Installation

All the drivers for the IMBAX-SP6 are available on IEI Resource Download Center (https://download.ieiworld.com). Type IMBAX-SP6 and press Enter to find all the relevant software, utilities, and documentation.

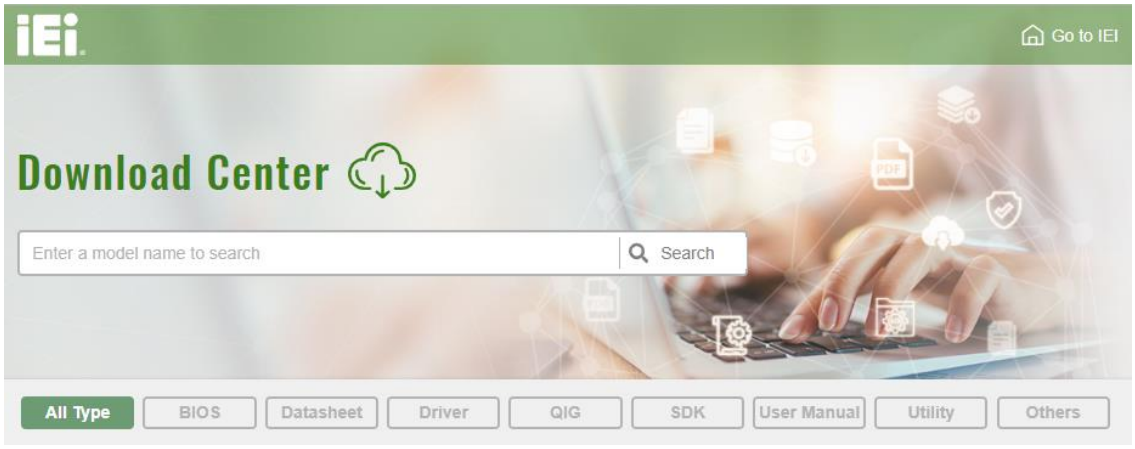
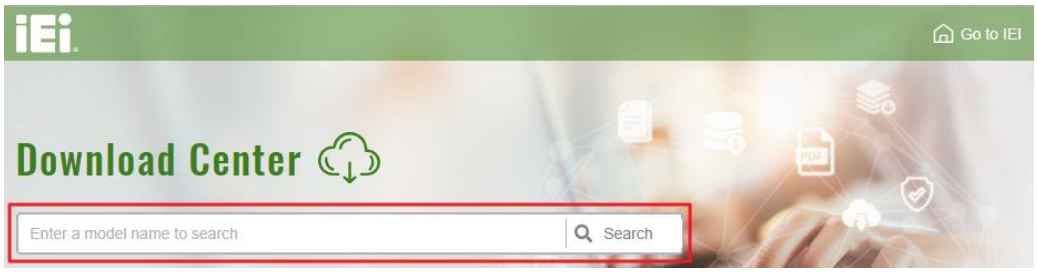


Figure 4-9: IEI Resource Download Center

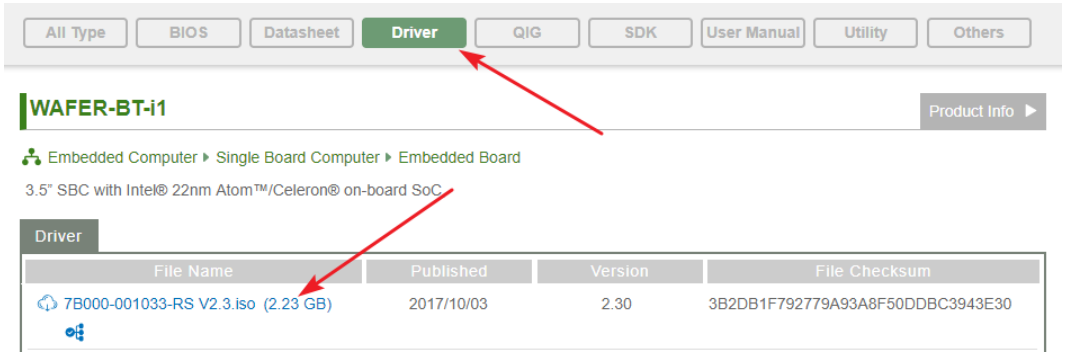
4.8.1 Driver Download

To download drivers from IEI Resource Download Center, follow the steps below.

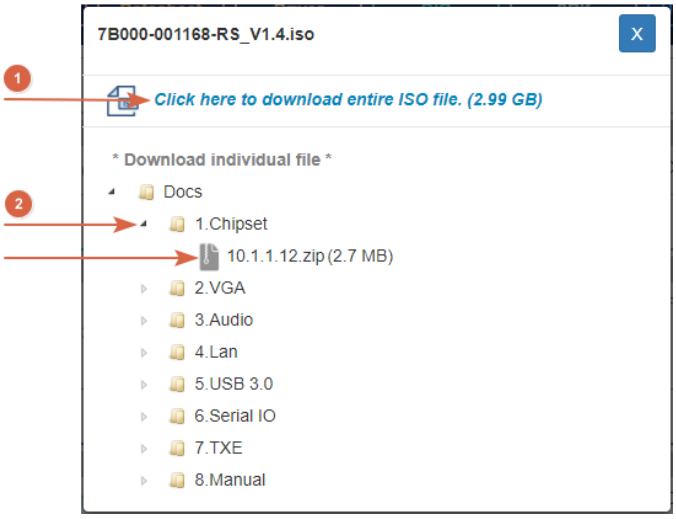
Step 1: Go to https://download.ieiworld.com. Type IMBAX-SP6 and press Enter.



Step 2: All product-related software, utilities, and documentation will be listed. You can choose **Driver** to filter the result.



Step 3: Click the driver file name on the page and you will be prompted with the following window. You can download the entire ISO file (❶), or click the small arrow to find an individual driver and click the file name to download (❷).



NOTE:

To install software from the downloaded ISO image file in Windows 8, 8.1 or 10, double-click the ISO file to mount it as a virtual drive to view its content. On Windows 7 system, an additional tool (such as Virtual CD-ROM Control Panel from Microsoft) is needed to mount the file.

Chapter

5

BIOS

5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.

NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

5.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. **Using keyboard**: Press the **DEL** or **F2** as soon as the system is turned on.
2. **Using touchscreen**: Press the **Setup** button on the upper right corner of the BIOS Starting Menu.

If the message disappears before the **DEL or F2** key is pressed, restart the computer and try again, then the BIOS Starting Menu will appear. Select "Setup" and press Enter to get into the BIOS Setup.

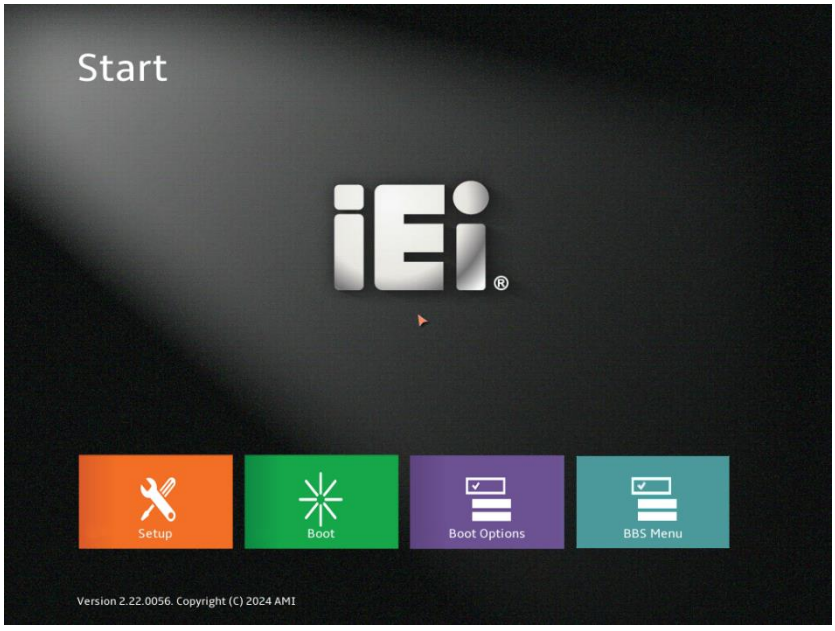


Figure 5-1: BIOS Starting Menu

5.1.2 Using Setup

The BIOS Setup menu can be navigated by using a keyboard or a touchscreen.

5.1.2.1 Keyboard Navigation

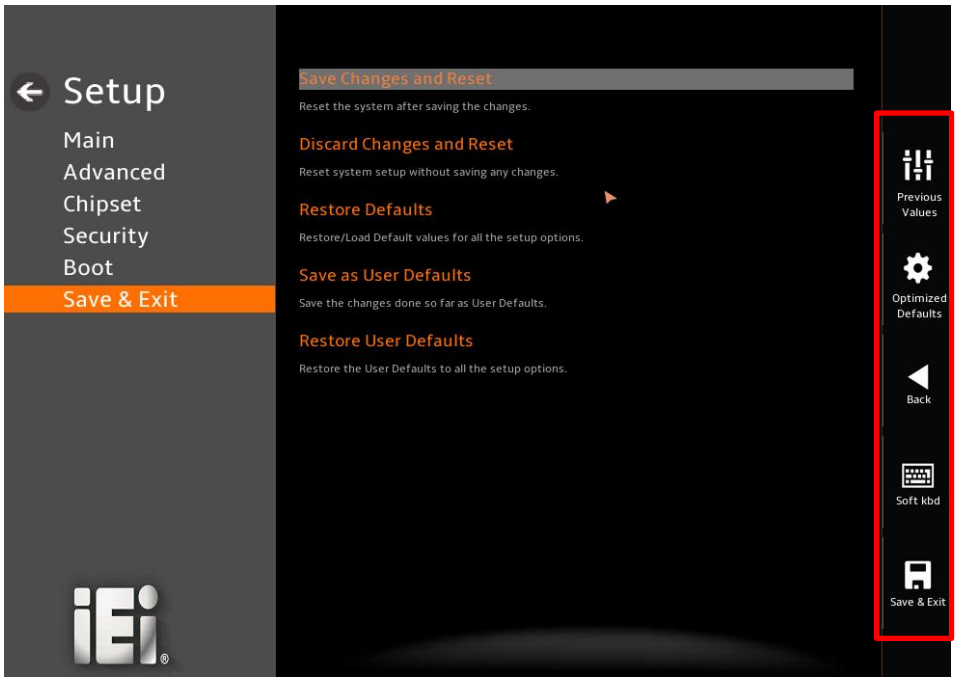
For keyboard navigation, use the navigation keys shown in **Table 5-1**.

Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
+	Increase the numeric value or make changes
-	Decrease the numeric value or make changes
Page Up	Move to the previous page
Page Dn	Move to the next page
Esc	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
F1	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2	Load previous values
F3	Load optimized defaults
F4	Save changes and Exit BIOS
<K>	Scroll help area upwards
<M>	Scroll help area downwards

Table 5-1: BIOS Navigation Keys

5.1.2.2 Touch Navigation

For touchscreen navigation, use the on-screen navigation keys shown below.



On-screen Button	Function
Previous Values	Load the last value you set.
Optimized Defaults	Load the factory default values in order to achieve the best performance.
Back	Return to the previous menu.
Soft kbd	Display the on-screen keyboard.
Save & Exit	Save the changes made to the BIOS options and reset the system.

Table 5-2: BIOS On-screen Navigation Keys

5.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window, press the **Esc** key.

5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the clear CMOS button described in **Chapter 4**.

5.1.5 BIOS Menu Bar

The **menu bar** on top of the BIOS screen has the following main items:

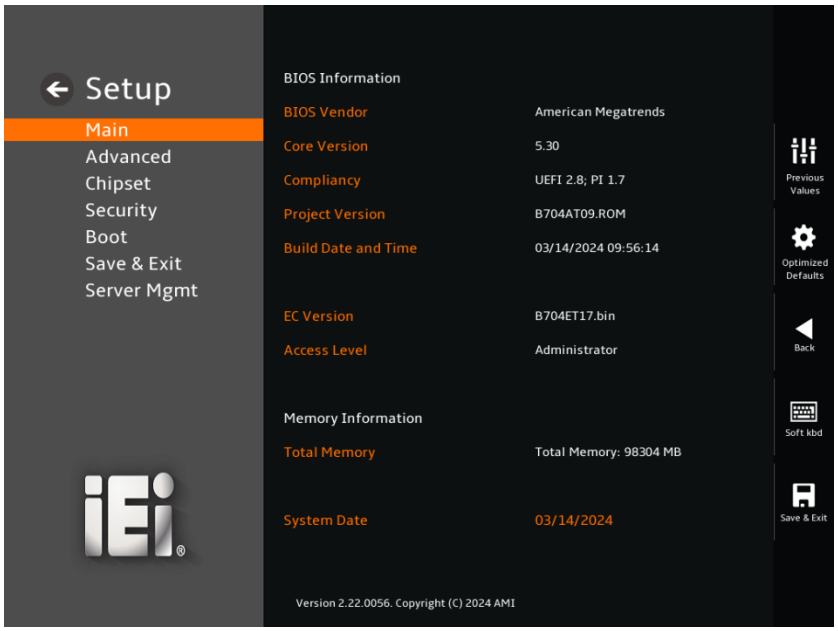
- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Security – Sets User and Supervisor Passwords.
- Boot – Changes the system boot configuration.
- Save & Exit – Selects exit options and loads default settings
- Server Mgmt – View the server management status and change the settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

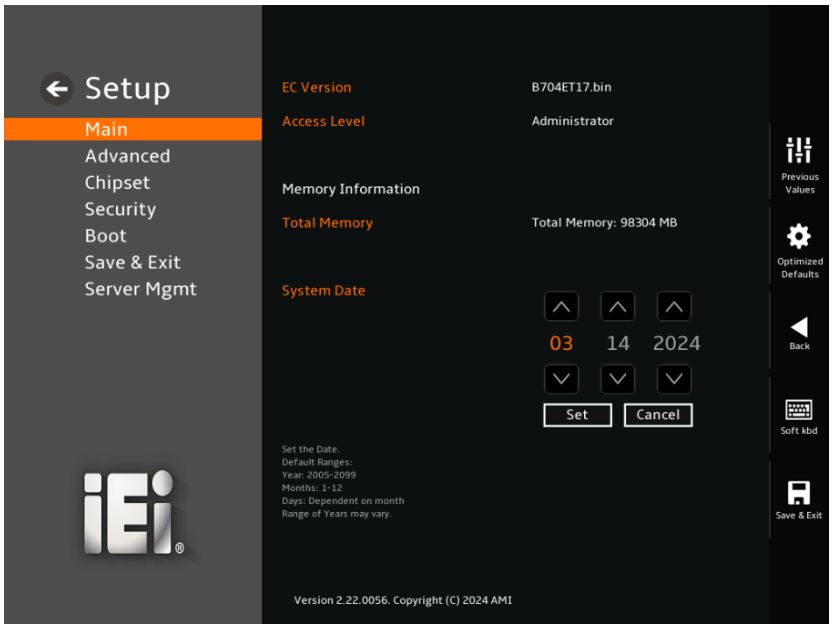
5.2 Main

The **Main** BIOS menu (**BIOS Menu 2**) appears when the **BIOS Setup** program is entered.

The **Main** menu gives an overview of the basic system information.



BIOS Menu 1: Main (1/5)



BIOS Menu 2: Main (2/5)

➔ **BIOS Information**

The **BIOS Information** lists a brief summary of the BIOS. The fields in **BIOS Information** cannot be changed. The items shown in the system overview include:

- **BIOS Vendor:** Installed BIOS vendor
- **Core Version:** Current BIOS version
- **Compliancy:** Current UEFI & PI version
- **Project Version:** the board version
- **Build Date and Time:** Date the current BIOS version was made
- **EC Version:** Current EC version

➔ **Memory Information**

The **Memory Information** lists a brief summary of the on-board memory. The fields in **Memory Information** cannot be changed.

- **Total Memory**: Displays the auto-detected system memory size and type.

➔ **System Date [xx/xx/xx]**

Use the **System Date** option to set the system date. Click the up and down arrows to adjust the day, month and year. Click **Set** to save the setting.

➔ **System Time [xx:xx:xx]**

Use the **System Time** option to set the system time. Click the up and down arrows to adjust the hours, minutes and seconds. Click **Set** to save the setting.

5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 3**) to configure the CPU and peripheral devices through the following sub-menus:

WARNING!

Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.

BIOS Menu 3: Advanced

5.3.1 Trusted Computing

Use the **Trusted Computing** menu (**BIOS Menu 4**) to configure settings related to the Trusted Computing Group (TCG) Trusted Platform Module (TPM).

BIOS Menu 4: Trusted Computing

➔ **Security Device Support [Disable]**

Use the **Security Device Support** option to enable or disable BIOS support for security device.

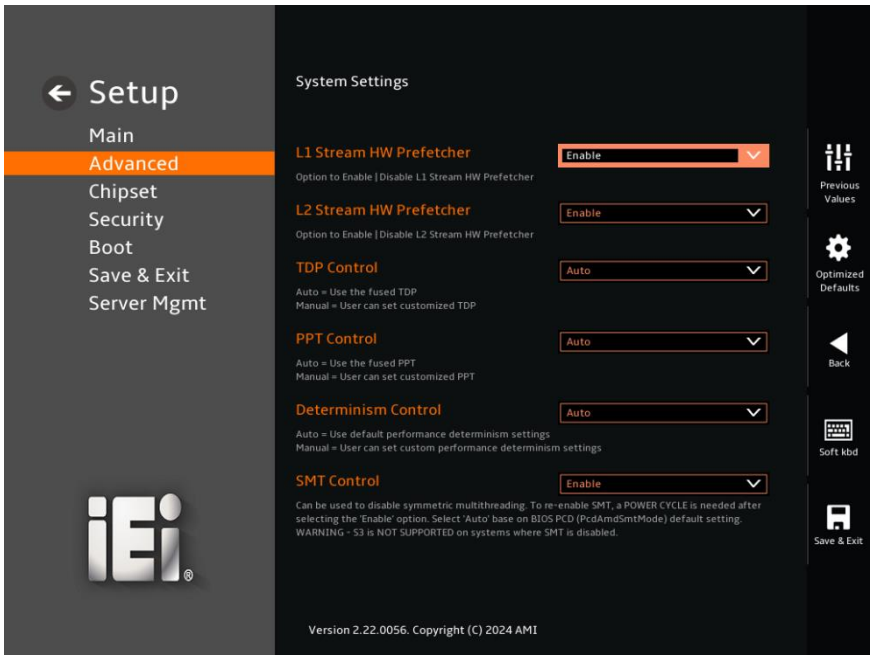
➔ **Disable** **DEFAULT** TPM support is disabled.

➔ **Enable** TPM support is enabled.

5.3.2 AMD CBS

Use the **AMD CBS** menu (**BIOS Menu 5**) to view detailed CPU specifications and configure the CPU settings.

BIOS Menu 5: AMD CBS



BIOS Menu 6: AMD CBS – System Settings

➔ **L1 Stream HW Prefetcher [Enabled]**

Use the **L1 Stream HW Prefetcher** option to enable or disable L1 Stream HW Prefetcher.

➔ **Disabled**		Disables L1 Stream HW Prefetcher.
➔ **Enabled**	**DEFAULT**	Enables L1 Stream HW Prefetcher.

➔ **L2 Stream HW Prefetcher [Enabled]**

Use the **L2 Stream HW Prefetcher** option to enable or disable L2 Stream HW Prefetcher.

➔ **Disabled**		Disables L2 Stream HW Prefetcher.
➔ **Enabled**	**DEFAULT**	Enables L2 Stream HW Prefetcher.

➔ **TDP Control [Auto]**

Use the **TDP Control** option to configure TDP.

➔ **Manual**		Use the fused TDP.
➔ **Auto**	**DEFAULT**	Users can set customized TDP.

➔ **PPT Control [Auto]**

Use the **PPT Control** option to configure PPT.

➔ **Manual**		Use the fused PPT.
➔ **Auto**	**DEFAULT**	Users can set customized PPT.

➔ **Determinism Control [Auto]**

Use the **Determinism Control** option to configure performance determinism settings.

➔ **Manual**		Use default performance determinism settings
➔ **Auto**	**DEFAULT**	Users can set custom performance determinism settings

➔ **SMT Control [Enabled]**

Use the **SMT Control** option to enable or disable symmetric multithreading. To re-enable SMT, a power cycle is needed after selecting the “Enable” option. **Warning: S3 is Not Supported on system where SMT is disabled.**

➔ **Disabled**		Disables symmetric multithreading
➔ **Enabled**	**DEFAULT**	Enables symmetric multithreading

➔ **Global C-state Control [Disabled]**

Use the **Global C-state Control** option to enable or disable IO-based C-state generation and DC C-states.

➔ **Disabled**	**DEFAULT**	Disables CPU power management
➔ **Enabled**		Enables CPU power management

➔ **Local APIC Mode [x2APIC]**

Use the **Local APIC Mode** option to set the mode of the APIC (Advanced Programmable Interrupt Controller).

➔ **Compatibility**		Set to compatibility mode
➔ **xAPIC**		Set to xAPIC mode
➔ **X2APIC**	**DEFAULT**	Set to x2APIC mode

➔ **ACPI SRAT L3 Cache As NUMA Domain [Disabled]**

Use the **ACPI SRAT L3 Cache As NUMA Domain** option to controls whether each L3 cache on the processor is treated as a separate NUMA domain.

➔ **Disabled**	**DEFAULT**	Memory addressing / NUMA nodes per socket will be declared
➔ **Enabled**		Each CCX in the system will be declared as a separate NUMA domain.

➔ **NUMA Nodes Per Socket [Auto]**

Use the **NUMA Nodes Per Socket** BIOS option to specify the number of desired NUMA nodes per socket. Zero will attempt to interleave the two sockets together. Configuration options are listed below:

- NPS0
- NPS1
- NPS2
- NPS4
- Auto **DEFAULT**

➔ **IOMMU [Enabled]**

Use the **IOMMU** option to enable or disable IOMMU (Input/Output Memory Management Unit).

➔ **Disabled**		Disables IOMMU
➔ **Enabled**	**DEFAULT**	Enables IOMMU

➔ **PCIe Ten Bit Tag Support [Disabled]**

Use the **PCIe Ten Bit Tag Support** option to enable or disable PCIe ten bit tags for the supported devices.

➔ **Disabled**	**DEFAULT**	Disables PCIe ten bit tags for the supported devices
➔ **Enabled**		Enables PCIe ten bit tags for the supported devices

➔ **APBDIS [0]**

The **APBDIS** is an option disabling CPU power state switching, which forces the CPU to run at its highest performance state.

➔ **0**	**DEFAULT**	Disables APBDIS (CPU dynamically adjusts its power state (P-states))
➔ **1**		Enables APBDIS (forces the CPU to constantly run at its highest performance state)

➔ **DRAM Scrub Time [24 hours]**

Use the **DRAM Scrub Time** option to configure the interval between DRAM scrubbing cycles. Configuration options are listed below:

- Disabled
- 1 hour
- 4 hours
- 6 hours
- 8 hours
- 12 hours
- 16 hours
- 24 hours **DEFAULT**
- 48 hours

➔ **(DRAM) Power Down Enable [Enabled]**

Use the **(DRAM) Power Down Enable** option to configure whether the main memory (DRAM) can enter low-power states when not actively in use.

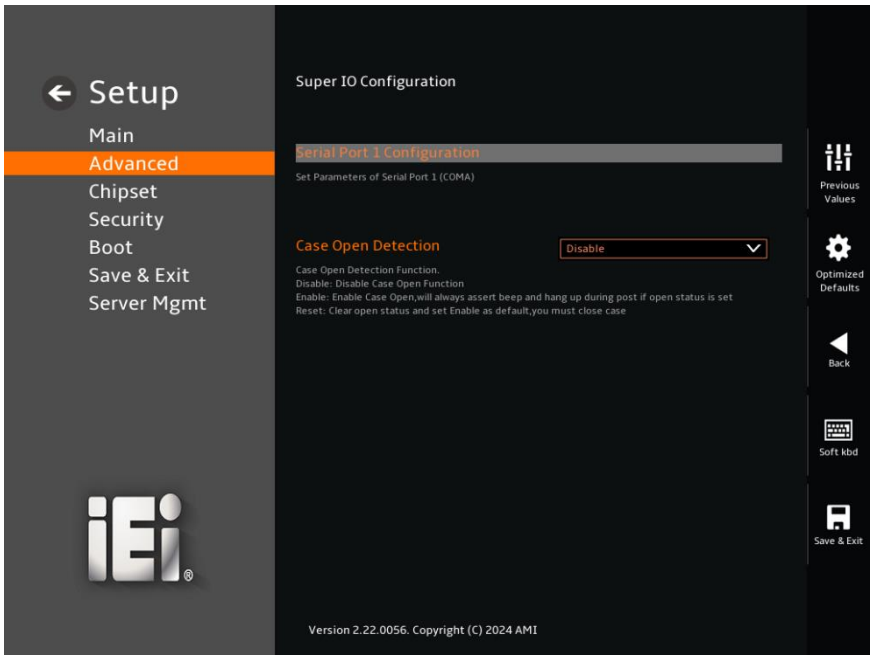
➔ **Disabled**		Disables DRAM power down mode
➔ **Enabled**	**DEFAULT**	Enables DRAM power down mode

➔ **ACPI CST C2 Latency [800]**

Enter a decimal number (unit: microseconds). Large C2 latency values will reduce the number of C2 transitions and reduce C2 residency. Fewer transitions can help when performance is sensitive to the latency of C2 entry and exit. Higher residency can improve performance by allowing higher frequency boost and reduce idle core power. With Linux kernel 6.0 or later, the C2 transition cost is significantly reduced. The best value will be dependent on kernel version, use case and workload.

5.3.3 Super IO Configuration

Use the **Super IO Configuration** menu (**BIOS Menu 7**) to set or change the configurations for serial ports.



BIOS Menu 7: Super IO Configuration

➔ **Case Open Detection [Disable]**

Use the **Case Open Detection** option to enable or disable Case Open Detection function.

➔ **Disabled**	**DEFAULT**	Disables Case Open Detection function.
➔ **Enabled**		Enables Case Open Detection function, and always assert beep and hang up during post if open status is set.
➔ **Reset**		Clear open status and set Enable as default, you must close case.

5.3.3.1 Serial Port 1 Configuration

Use the **Serial Port 1 Configuration** menu (**BIOS Menu 8**) to configure the serial port.

BIOS Menu 8: Serial Port 1 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

➔ **Disabled**		Disable the serial port
➔ **Enabled**	**DEFAULT**	Enable the serial port

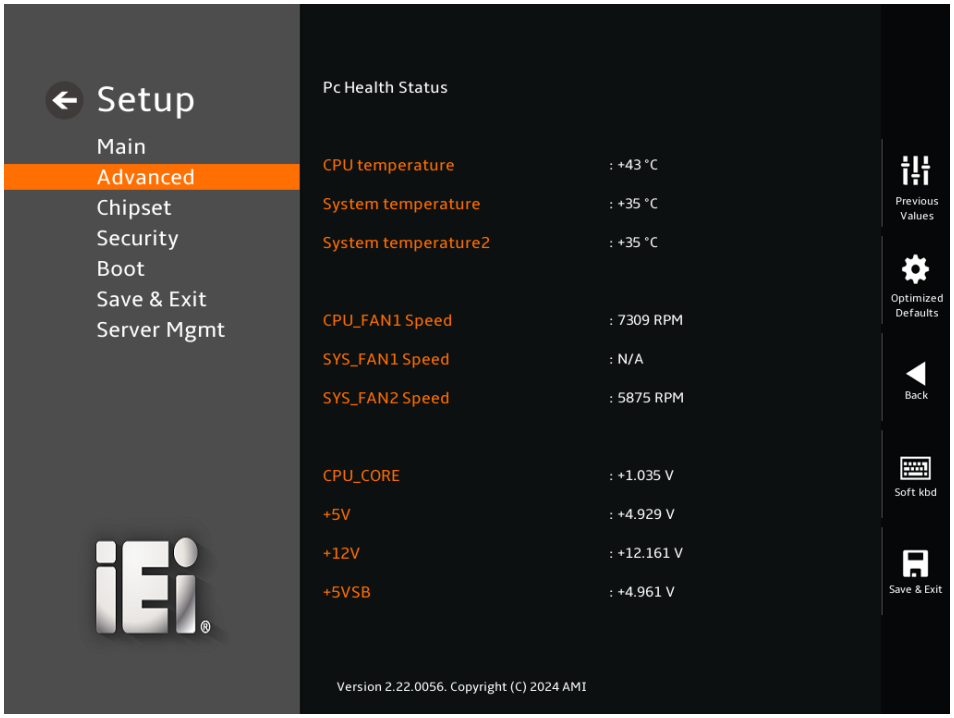
➔ **Device Settings**

The **Device Settings** option shows the serial port IO port address and interrupt address.

➔ **IO=3F8h; IRQ=4** Serial Port I/O port address is 3F8h and the interrupt address is IRQ4

5.3.4 IT5571 H/W Monitor

The **IT5571 H/W Monitor** menu (**BIOS Menu 9**) contains the smart fan mode configuration submenu and shows the state of H/W real-time operating temperature, fan speeds and system voltages.



BIOS Menu 9: IT5571 H/W Monitor

➔ **PC Health Status**

The following system parameters and values are shown. The system parameters that are monitored are:

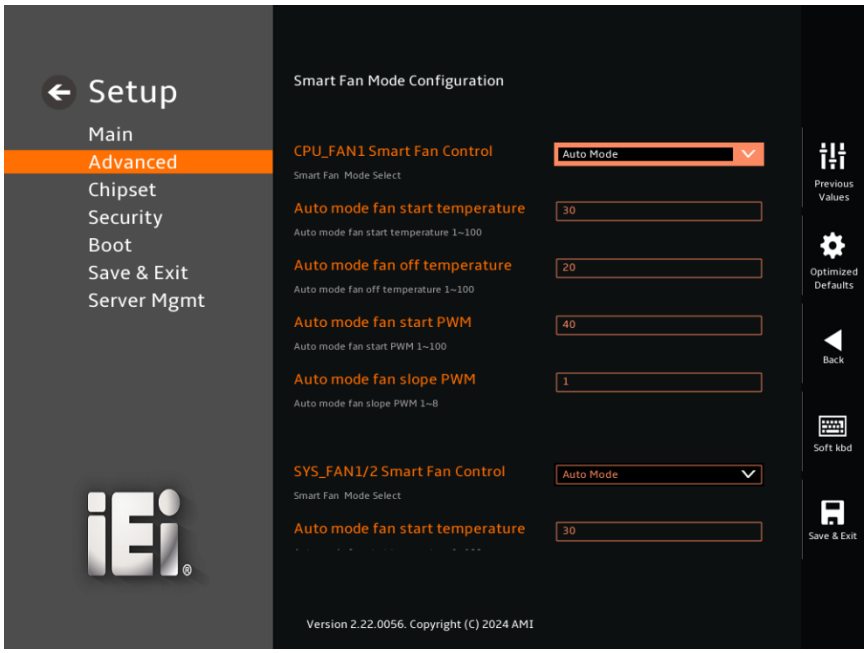
- System Temperatures:
  - CPU Temperature

- System Temperature
- System Temperature 2

- Fan Speeds:
  - CPU_Fan1 speed
  - SYS_Fan1 speed
  - SYS_Fan2 speed
- Voltages:
  - CPU_CORE
  - +5V
  - +12V
  - +5VSB
  - +3.3V
  - +3.3VSB
  - CPU_CORE2

5.3.4.1 Smart Fan Mode Configuration

Use the **Smart Fan Mode Configuration** submenu (**BIOS Menu 10**) to configure the CPU/system fan start/off temperature and control mode.



BIOS Menu 10: Smart Fan Mode Configuration (1/2)

BIOS Menu 11: Smart Fan Mode Configuration (2/2)

➔ **CPU_FAN1 Smart Fan Control [Auto Mode]**

Use the **CPU_FAN1 Smart Fan Control** option to configure the CPU Smart Fan.

➔ **Manual Mode**		The fan spins at the speed set in Manual Mode settings.
➔ **Auto Mode**	**DEFAULT**	The fan adjusts its speed using Auto Mode settings.

➔ **SYS_FAN1/2 Smart Fan Control [Auto Mode]**

Use the **SYS_FAN1/2 Smart Fan Control** option to configure the System Smart Fan.

➔ **Manual Mode**		The fan spins at the speed set in Manual Mode settings.
➔ **Auto Mode**	**DEFAULT**	The fan adjusts its speed using Auto Mode settings.

➔ **Auto mode fan start/off temperature**

Use the + or – key to change the **Auto mode fan start/off temperature** value. Enter a decimal number between 1 and 100.

➔ **Auto mode fan start PWM**

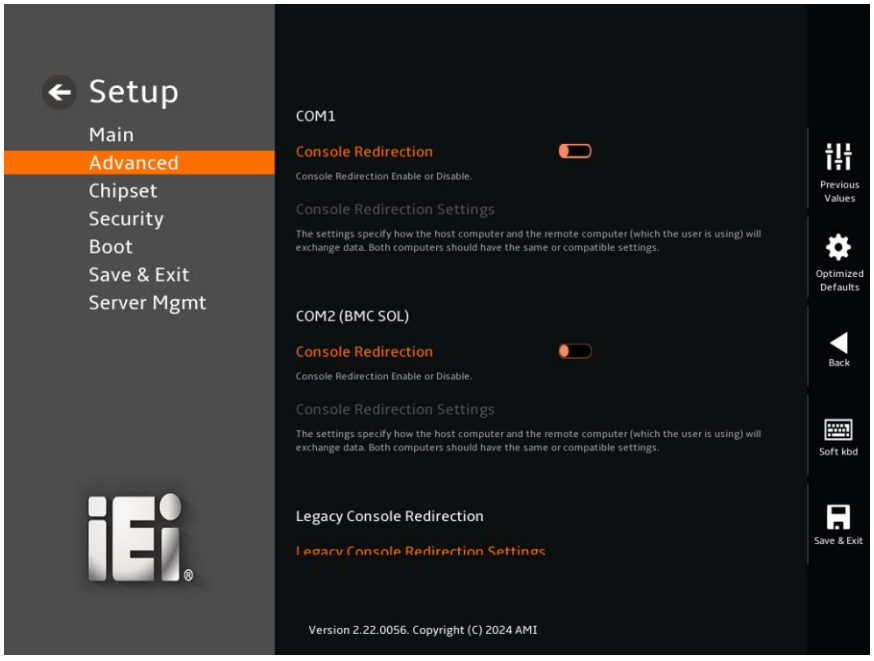
Use the + or – key to change the **Auto mode fan start PWM** value. Enter a decimal number between 1 and 100.

➔ **Auto mode fan slope PWM**

Use the + or – key to change the **Auto mode fan slope PWM** value. Enter a decimal number between 1 and 8.

5.3.5 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 12**) allows the console redirection options to be configured. Console Redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.



BIOS Menu 12: Serial Port Console Redirection

➔ **Console Redirection [Disabled]**

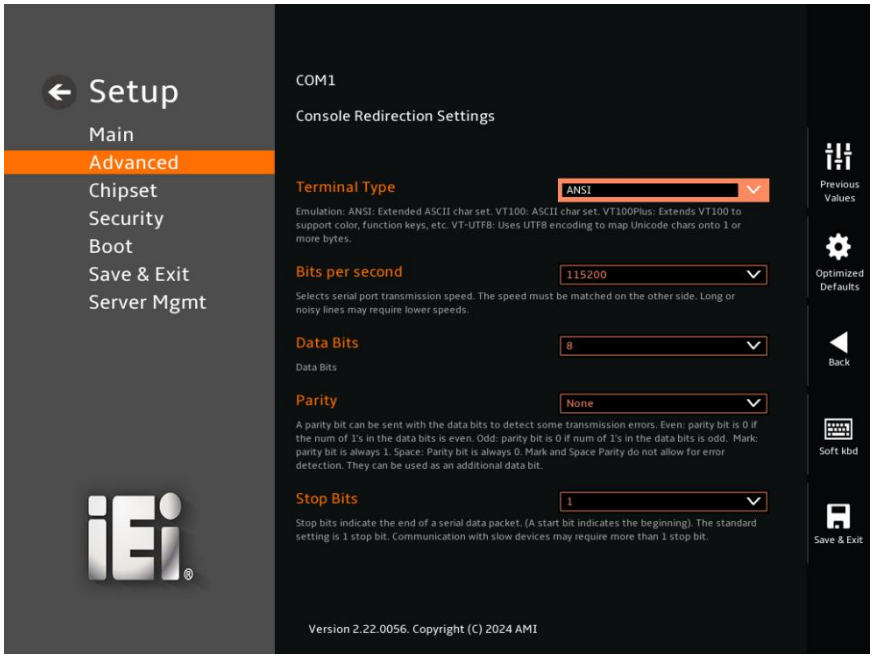
Use **Console Redirection** option to enable or disable the console redirection function.

➔	**Disabled**	**DEFAULT**	Disabled the console redirection function
➔	**Enabled**		Enabled the console redirection function

The **Console Redirection Settings** submenu will be available when the **Console Redirection** option is enabled.

5.3.5.1 Console Redirection Settings

The following options are available in the **Console Redirection Settings** submenu (**BIOS Menu 13**) when the **COM Console Redirection** option is enabled.



BIOS Menu 13: COM Console Redirection Settings

➔ **Terminal Type [ANSI]**

Use the **Terminal Type** option to specify the remote terminal type.

➔ **VT100**		The target terminal type is VT100
➔ **VT100Plus**		The target terminal type is VT100+
➔ **VT-UTF8**		The target terminal type is VT-UTF8
➔ **ANSI**	**DEFAULT**	The target terminal type is ANSI

➔ **Bits per second [115200]**

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match on the other side. Long or noisy lines may require lower speeds.

➔ **9600**		Sets the serial port transmission speed at 9600.
➔ **19200**		Sets the serial port transmission speed at 19200.
➔ **38400**		Sets the serial port transmission speed at 38400.
➔ **57600**		Sets the serial port transmission speed at 57600.
➔ **115200**	**DEFAULT**	Sets the serial port transmission speed at 115200.

➔ **Data Bits [8]**

Use the **Data Bits** option to specify the number of data bits.

➔ **7**		Sets the data bits at 7.
➔ **8**	**DEFAULT**	Sets the data bits at 8.

➔ **Parity [None]**

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

➔ **None**	**DEFAULT**	No parity bit is sent with the data bits.
➔ **Even**		The parity bit is 0 if the number of ones in the data bits is even.

➔	**Odd**	The parity bit is 0 if the number of ones in the data bits is odd.
➔	**Mark**	The parity bit is always 1. This option does not allow for error detection.
➔	**Space**	The parity bit is always 0. T This option does not allow for error detection.

➔ **Stop Bits [1]**

Use the **Stop Bits** option to specify the number of stop bits used to indicate the end of a serial data packet. Communication with slow devices may require more than 1 stop bit.

➔	**1**	**DEFAULT**	Sets the number of stop bits at 1.
➔	**2**		Sets the number of stop bits at 2.

5.3.6 CPU Configuration

The **CPU Configuration** menu (**BIOS Menu 15**) configures CPU parameters.

BIOS Menu 14: CPU Configuration

➔ **SVM Mode [Enabled]**

Use the **SVM Mode** option to enable or disable CPU virtualization.

➔	**Disabled**		Disable CPU virtualization
➔	**Enabled**	**DEFAULT**	Enable CPU virtualization

➔ **Node 0 Information [Enabled]**

Enter the **Node 0 Information** submenu to view memory information related to Node 0.

5.3.7 Network Stack Configuration

The **Network Stack Configuration** menu (**BIOS Menu 15**) configures network stack settings.

BIOS Menu 15: Network Stack Configuration

➔ **Network Stack [Disabled]**

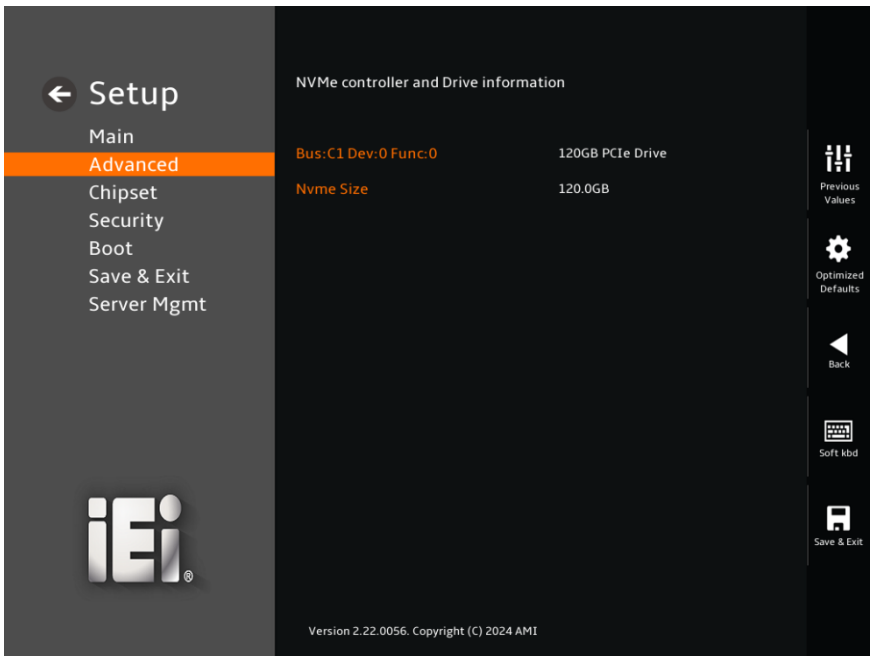
Use the **Network Stack** option to enable or disable UEFI network stack.

➔ **Disabled** **DEFAULT** Disable UEFI network stack

➔ **Enabled** Enable UEFI network stack

5.3.8 NVMe Configuration

Use the **NVMe Configuration** (**BIOS Menu 16**) menu to display the NVMe controller and device information.



BIOS Menu 16: NVMe Configuration

5.3.9 SATA Configuration

Use the **SATA Configuration** menu (**BIOS Menu 17**) to change and/or set the configuration of the SATA devices installed in the system.

BIOS Menu 17: SATA Configuration

5.4 Chipset

Use the **Chipset** menu (**BIOS Menu 18**) to access the PCH IO and System Agent (SA) configuration menus.

WARNING!

Setting the wrong values for the Chipset BIOS selections in the Chipset BIOS menu may cause the system to malfunction.

BIOS Menu 18: Chipset

5.4.1 South Bridge

Use the **South Bridge** menu (**BIOS Menu 19**) to configure the South Bridge parameters.

BIOS Menu 19: South Bridge

➔ **Auto Power Button Function [Disabled (ATX)]**

The **Auto Power Button Function** BIOS option shows the power mode state set by the onboard **J_ATX_AT1** switch.

➔ **Restore AC Power Loss [Last State]**

Use the **Restore AC Power Loss** BIOS option to specify what state the system returns to if there is a sudden loss of power to the system when the power mode is ATX.

➔ **Power Off**		The system remains turned off
➔ **Power On**		The system turns on
➔ **Last State**	**DEFAULT**	The system returns to its previous state. If it was on, it turns itself on. If it was off, it remains off.

➔ **USB Power [+5V DUAL]**

Use the **USB Power** BIOS option to configure the USB power source for the corresponding USB connectors.

➔ **+5V DUAL** **DEFAULT** Sets the USB power source to +5V dual

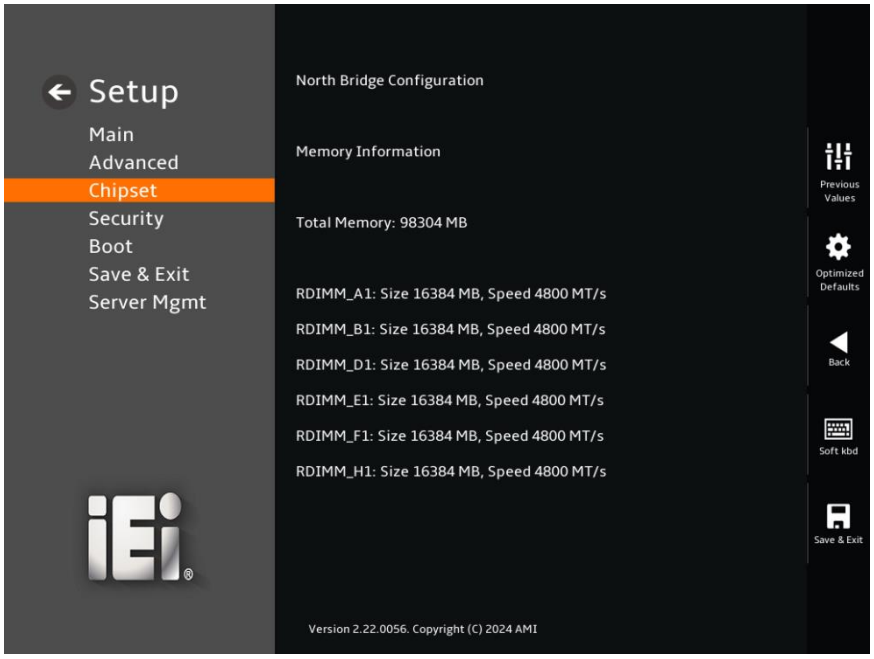
➔ **+5V** Sets the USB power source to +5V

BIOS Options	Configured USB Ports
USB Power SW1	IPMILAN-USB1B (external USB 3.2 Gen 1 ports)
USB Power SW2	COM1_USB1B (external USB 3.2 Gen 1 ports)

Table 5-3: BIOS Options and Configured USB Ports

5.4.2 North Bridge

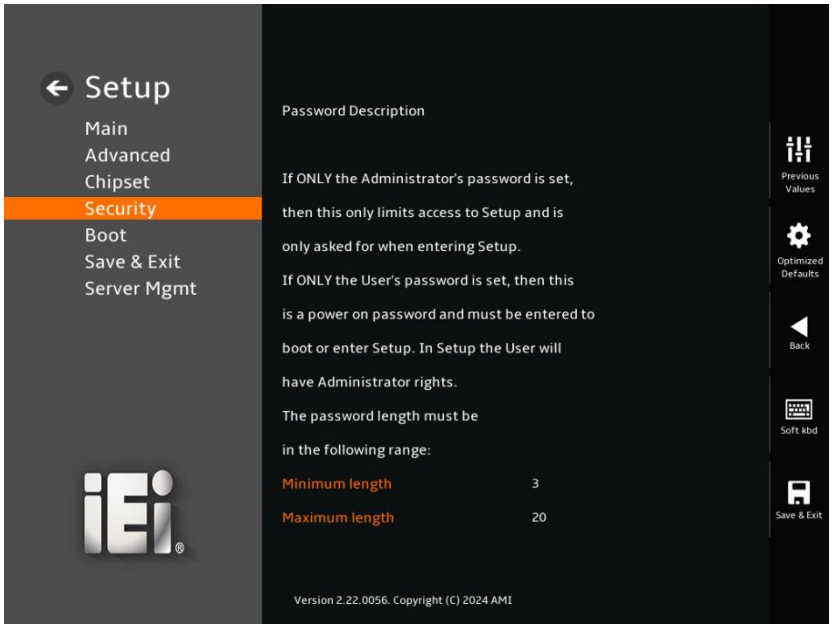
Use the **North Bridge** menu (**BIOS Menu 20**) to view the North Bridge parameters.



BIOS Menu 20: North Bridge

5.5 Security

Use the **Security** menu (**BIOS Menu 21)** to set system and user passwords.



BIOS Menu 21: Security

➔ **Administrator Password**

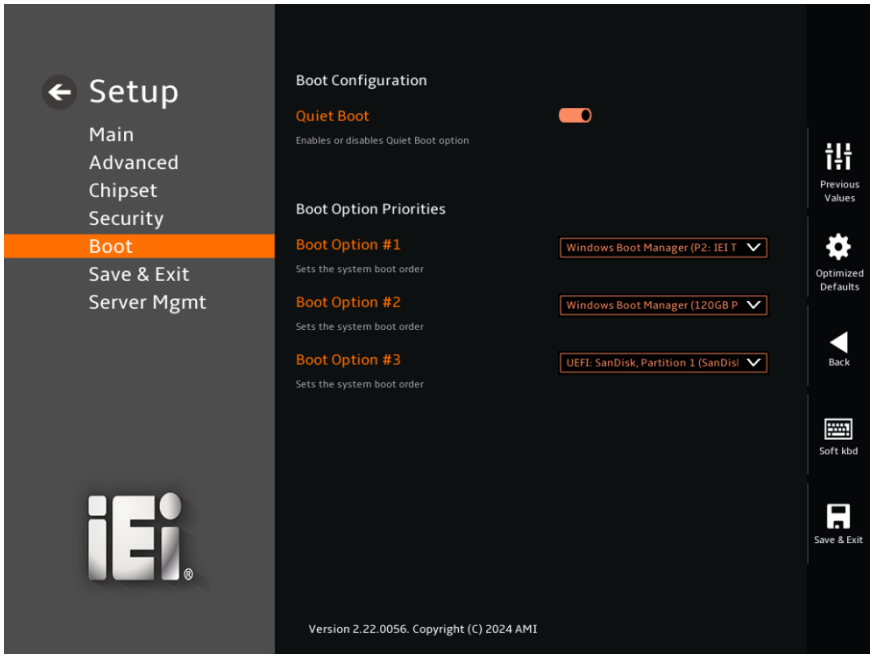
Use the **Administrator Password** to set or change an administrator password.

➔ **User Password**

Use the **User Password** to set or change a user password.

5.6 Boot

Use the **Boot** menu (**BIOS Menu 22**) to configure system boot options.



BIOS Menu 22: Boot

➔ **Quiet Boot [Enabled]**

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

➔	**Disabled**		Normal POST messages displayed
➔	**Enabled**	**DEFAULT**	OEM Logo displayed instead of POST messages

5.6.1 Boot Option Priorities

Use the Boot Option # N to choose the system boots from the peripherals you selected.

5.7 Save & Exit

Use the **Save & Exit** menu (**BIOS Menu 23**) to load default BIOS values, optimal failsafe values and to save configuration changes.

BIOS Menu 23: Save & Exit

➔ **Save Changes and Reset**

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and reset the system.

➔ **Discard Changes and Reset**

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

➔ **Restore Defaults**

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

➔ **Save as User Defaults**

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

➔ **Restore User Defaults**

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

5.8 Server Management

Use the **Server Management** menu (**BIOS Menu 24**) to display the server management status and change the settings.

BIOS Menu 24: Server Management

➔ **BMC Support [Enabled]**

Use the **BMC Support** option to enable or disable the interfaces to communicate with BMC.

➔ **Enabled**	**DEFAULT**	Enables the interfaces to communicate with BMC.
➔ **Disabled**		Disables the interfaces to communicate with BMC.

5.8.1 BMC Network Configuration

Use the **BMC Network Configuration** menu (**BIOS Menu 25**) to configure the BMC network parameters.

BIOS Menu 25: BMC Network Configuration

5.8.1.1 LAN Channel (IPV4)

➔ **Configuration Address Source [Unspecified]**

Use the **Configuration Address Source** option to select the BMC network address source.

➔ **Unspecified** **DEFAULT** Does not modify any BMC network parameters during BIOS phase

➔ **Static**	Manually sets the BMC network parameters. If this option is selected, the following items will be configurable: *Station IP address *Subnet mask *Router IP address *Router MAC address
➔ **DynamicBmcDhcp**	Obtains BMC network parameters by BMC dynamically.
➔ **DynamicBmcNonDhcp**	Loads BMC network parameters by BIOS.

5.8.1.2 LAN Channel (IPV6)

➔ **IPv6 Support [Disabled]**

Use the **IPv6 Support** option to enable or disable the IPv6 protocol.

➔ **Disabled**	**DEFAULT**	Disables IPv6 Support
➔ **Enabled**		Enables IPv6 Support

Appendix

A

Regulatory Compliance

DECLARATION OF CONFORMITY

This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

FCC WARNING

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

B

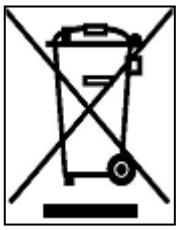
Product Disposal

CAUTION:

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

- Outside the European Union–If you wish to dispose of used electrical and electronic products outside the European Union, please contact your local authority so as to comply with the correct disposal method.
- Within the European Union–The device that produces less waste and is easier to recycle is classified as electronic device in terms of the European Directive 2012/19/EU (WEEE), and must not be disposed of as domestic garbage.



EU-wide legislation, as implemented in each Member State, requires that waste electrical and electronic products carrying the mark (left) must be disposed of separately from normal household waste. This includes monitors and electrical accessories, such as signal cables or power cords. When you need to dispose of your device, please follow the guidance of your local authority, or ask the shop where you purchased the product. The mark on electrical and electronic products only applies to the current European Union Member States.

Please follow the national guidelines for electrical and electronic product disposal.

Appendix

C

BIOS Options

Below is a list of BIOS configuration options in the BIOS chapter.

Appendix

D

Watchdog Timer

NOTE:

The following discussion applies to DOS environment. Contact IEI support or visit the IEI website for specific drivers for other operating systems.

The Watchdog Timer is provided to ensure that standalone systems can always recover from catastrophic conditions that cause the CPU to crash. This condition may have occurred by external EMIs or a software bug. When the CPU stops working correctly, Watchdog Timer either performs a hardware reset (cold boot) or a Non-Maskable Interrupt (NMI) to bring the system back to a known state.

A BIOS function call (INT 15H) is used to control the Watchdog Timer.

INT 15H:

AH – 6FH Sub-function:	
AL – 2:	Sets the Watchdog Timer's period.
BL:	Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup).

Table D-1: AH-6FH Sub-function

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. When the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

NOTE:

When exiting a program it is necessary to disable the Watchdog Timer, otherwise the system resets.

EXAMPLE PROGRAM:

```
; INITIAL TIMER PERIOD COUNTER

;
W_LOOP:
;

        MOV     AX, 6F02H       ;setting the time-out value
        MOV     BL, 30          ;time-out value is 48 seconds
        INT     15H

;
; ADD THE APPLICATION PROGRAM HERE
;

        CMP     EXIT_AP, 1      ;is the application over?
        JNE     W_LOOP          ;No, restart the application

        MOV     AX, 6F02H       ;disable Watchdog Timer
        MOV     BL, 0           ;
        INT     15H

;
; EXIT ;
```

Appendix

E

Error Beep Code

E.1 PEI Beep Codes

Number of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

E.2 DXE Beep Codes

Number of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

NOTE:

If you have any question, please contact IEI for further assistance.

Appendix

F

Hazardous Materials Disclosure

F.1 RoHS II Directive (2015/863/EU)

The details provided in this appendix are to ensure that the product is compliant with the RoHS II Directive (2015/863/EU). The table below acknowledges the presences of small quantities of certain substances in the product, and is applicable to RoHS II Directive (2015/863/EU).

Please refer to the following table.

Part Name	Toxic or Hazardous Substances and Elements									
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)	Bis(2-ethylhexyl) phthalate (DEHP)	Butyl benzyl phthalate (BBP)	Dibutyl phthalate (DBP)	Diisobutyl phthalate (DIBP)
Housing	O	O	O	O	O	O	O	O	O	O
Printed Circuit Board	O	O	O	O	O	O	O	O	O	O
Metal Fasteners	O	O	O	O	O	O	O	O	O	O
Cable Assembly	O	O	O	O	O	O	O	O	O	O
Fan Assembly	O	O	O	O	O	O	O	O	O	O
Power Supply Assemblies	O	O	O	O	O	O	O	O	O	O
Battery	O	O	O	O	O	O	O	O	O	O

O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in Directive (EU) 2015/863.

X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in Directive (EU) 2015/863.

F.2 China RoHS

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有"环境友好使用期限"的标签，此期限是估算这些物质"不会有泄漏或突变"的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
壳体	O	O	O	O	O	O
印刷电路板	O	O	O	O	O	O
金属螺帽	O	O	O	O	O	O
电缆组装	O	O	O	O	O	O
风扇组装	O	O	O	O	O	O
电力供应组装	O	O	O	O	O	O
电池	O	O	O	O	O	O

O: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求。