# Mustang FPGA download Cable User Guide





#### **Install Quartus tool**

- cd /home/iei/Downloads/
- sudo chmod +x QuartusProProgrammerSetup-18.1.1.263-linux.run
- sudo ./QuartusProProgrammerSetup-18.1.1.263-linux.run
- Installation Directory:
  - /home/iei/intelFPGA\_pro/18.1



#### **Connect FPGA Download Cable**

 It is mandatory for user to implement FPGA programmer kit to update FPGA bitstreams if your target OpenVINO toolkit version does not match the Mustang-F100-A10 card's bitstreams.



# **FPGA Download Cable Ordering info**

Please visit IEI website to purchase FPGA download cable Item No. : 7Z000-00FPGA00

https://www.ieiworld.com/en/product/model.php?II=614

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Overview	Features	Specifications	Marketing Materials	News	
		Ordering Info			
Item No.	Descri	ption			
7Z000-00FPGA00 OTHERS PEI Download+U		RS PERIPHERAL DEVICE;FPGA Dow and+USB CABLE+IDE CABLE+FPGA	ERIPHERAL DEVICE;FPGA Download Cable;IEI USB DOWNLOAD CABLE;Macnica;USB USB CABLE+IDE CABLE+FPGA CABLE		
Mustang-F100-A10-R10		PCIe FPGA Highest Performance Accelerator Card with Arria 10 1150GX support DDR4 2400Hz 8GB, PCIe Gen3 x8 interface			

## **Install BSP Update tool**

- cd /home/iei/Downloads/fpga\_support\_files
- source /home/iei/setup\_env.sh
- sudo mv config/blacklist-altera-cvp.conf /etc/modprobe.d
- sudo cp config/51-usbblaster.rules /etc/udev/rules.d/
- sudo udevadm control --reload-rules && udevadm trigger
- Isusb | grep Altera
- jtagconfig
- jtagconfig --getparam 1 JtagClock

#### Free Download:

FPGA driver:
 <a>http://registrationcenter-</a>
 <a>download.intel.com/akdlm/irc\_nas/129</a>
 <a>54/fpga\_support\_files.tgz</a>

## **Install BSP Update tool**



- cd /home/iei/Download/fpga\_support\_files
- source /home/iei/setup\_env.sh
- quartus\_pgm -c 1 -m JTAG -o
  "p;/home/iei/Downloads/fpga\_support\_files/config/hddlf/2019.r1/a10\_ 1150\_sg1/bringup/sg1\_boardtest\_2ddr\_base.sof"
- Reboot

iei@iei-SER0: ~/Downloads/fpga_support_files	11 <u>:23 ∛</u>
<pre>iei@iei-SER0:~\$ cd /home/iei/Downloads/fpga_support_files/ iei@iei-SER0:~/pownloads/fpga_support_files\$ source setup_env.sh Adding to Path (OpenVINO AOCL) Adding to Path (QT Pro)</pre>	
aoc was not found, but aocl was found. Assuming only RTE is installed.	
AOCL_BOARD_PACKAGE_ROOT is set to /opt/altera/aocl-pro-rte/aclrte-linux64/board/a10_1150_sg1. Using that. Adding /opt/altera/aocl-pro-rte/aclrte-linux64/bin to PATH Adding /opt/altera/aocl-pro-rte/aclrte-linux64/binst/linux64/lib to LD_LIBRARY_PATH Adding /opt/altera/aocl-pro-rte/aclrte-linux64/board/a10_1150_sg1/linux64/lib to LD_LIBRARY_PATH [setupvars.sh] OpenVINO environment initialized [setupvars.sh] openVINO environment initialized [setuptars.sh].openVINO.ads/fpga_support_files quartus_pgm -c 1 -m JTAG -o "p;/home/iei/Downloads/fpga_support_file r1/a10_1150_sg1/bringup/sg1_boardtest_2ddr_base.sof"	rs/config/hddlf/2019.
Info: Info: Running Quartus Prime Programmer Info: Version 18.1.1 Build 263 12/14/2018 SJ Pro Edition Info: Copyright (C) 2018 Intel Corporation. All rights reserved. Info: Your use of Intel Corporation's design tools, logic functions Info: and other software and tools, and any partner logic Info: functions, and any output files from any of the foregoing Info: (including device programming or simulation files), and any	
Info: associated documentation or information are expressly subject Info: to the terms and conditions of the Intel Program License Info: Subscription Agreement, the Intel Quartus Prime License Agreement, Info: the Intel FPGA IP License Agreement, or other applicable license Info: agreement, including, without limitation, that your use is for Info: the sole purpose of programming logic devices manufactured by Info: Intel and sold by Intel or its authorized distributors. Please Info: refer to the applicable agreement for further details, at	
Info: https://tpgasoftware.intel.com/euta. Info: Processing started: Fri May 31 11:21:40 2019 Info: Command: quartus_pgm -c 1 -m JTAG -o p;/home/iei/Downloads/fpga_support_files/config/hddlf/2019.r1/a10_1156	
Info (213045): Using programming cable "USB-Blaster [1-10]" Info (213041): Using programming file /home/iei/Downloads/fpga_support_files/config/hddlf/2019.r1/a10_1150_sg1/br 2ddr_base.sof with checksum 0x30A874E9 for device 10AX115H2F3401 Info (209060): Started Programmer operation at Fri May 31 11:21:47 2019	
Info (209016): Configuring device index 1 Info (209017): Device 1 contains JTAG ID code 0x02E660DD Info (209007): Configuration succeeded 1 device(s) configured Info (209011): Successfully performed operation(s)	
Info (209061): Ended Programmer operation at Fri May 31 11:22:57 2019 Info: Quartus Prime Programmer was successful. 0 errors, 0 warnings Info: Peak virtual memory: 2328 megabytes Info: Processing ended: Fri May 31 11:22:57 2019	
Info: Elapsed time: 00:01:17 iei@iei-SER0:~/Downloads/fpga_support_files\$	

- cd /home/iei/Downloads/fpga\_support\_files
- source /home/iei/Downloads/fpga\_support\_files/setup\_env.sh
- export QUARTUS\_ROOTDIR=/home/iei/intelFPGA\_pro/18.1/qprogramer/
- jtagconfig
- jtagconfig --getparam 1 JtagClock
  - Output: 6M
- cd config/aocl\_flash/linux64
- sudo cp -R perl /home/iei/intelFPGA\_pro/18.1/qprogramer/linux64/
- aocl diagnose
- aocl flash acl0 /opt/intel/openvino/bitstreams/a10\_vision\_design\_bitstreams/2019R1\_PL 1\_FP16\_ResNet\_SqueezeNet\_VGG\_ELU.aocx
- Poweroff

Bitstream				
FP11				
2019R1_PL1_FP11_AlexNet_GoogleNet				
2019R1_PL1_FP11_ELU				
2019R1_PL1_FP11_MobileNetCaffe				
2019R1_PL1_FP11_MobileNet_Clamp				
2019R1_PL1_FP11_ResNet_SqueezeNet_VG				
G				
2019R1_PL1_FP11_RMNet				
2019R1_PL1_FP11_SSD300_TinyYolo				
FP16				
2019R1_PL1_FP16_AlexNet_GoogleNet_SSD				
300_TinyYolo				
2019R1_PL1_FP16_MobileNet_Clamp				
2019R1_PL1_FP16_ResNet_SqueezeNet_VG				
G_ELU				
2019R1_PL1_FP16_RMNet				
OpenVINO 2019 R1 Bitstream with Topology				

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Call "aocl diagnose all" to run diagnose for all devices

iei@iei-SER0:~/Downloads/fpga\_support\_files/config/aocl\_flash/linux64\$ aocl flash acl0 /opt/intel/openvino/bitstreams/a10 a10 dcp bitstreams/ a10 devkit bitstreams/ a10 vision design bitstreams/ iei@iei-SER0:~/Downloads/fpga support files/config/aocl flash/linux64\$ aocl flash acl0 /opt/intel/openvino/bitstreams/a10 vision desi on bitstreams/2019R1 PL1 FP1 2019R1 PL1 FP11 AlexNet GoogleNet.aocx 2019R1 PL1 FP11 SSD300 TinyYolo.aocx 2019R1 PL1 FP11 ELU.aocx 2019R1\_PL1\_FP16\_AlexNet\_GoogleNet\_SSD300\_TinyYolo.aocx 2019R1 PL1 FP11 MobileNetCaffe.aocx 2019R1 PL1 FP16 MobileNet Clamp.aocx 2019R1 PL1 FP11 MobileNet Clamp.aocx 2019R1 PL1 FP16 ResNet SqueezeNet VGG ELU.aocx 2019R1 PL1 FP11 ResNet SqueezeNet VGG.aocx 2019R1 PL1 FP16 RMNet.aocx 2019R1 PL1 FP11 RMNet.aocx iei@iei-SER0:~/Downloads/fpga support files/config/aocl flash/linux64\$ aocl flash acl0 /opt/intel/openvino/bitstreams/a10 vision desi gn bitstreams/2019R1 PL1 FP16 ResNet SqueezeNet VGG ELU.aocx aocl flash: Running flash from /opt/altera/aocl-pro-rte/aclrte-linux64/board/a10 1150 sg1/linux64/libexec